Crystal Image through
Imaging Innovation

PIXELPLUS

Preliminary

Datasheet

FHD ISP with Multiple Standard HD Analog Transmitter

PI4008K

Rev 0.6

Last update : 27. Feb. 2019

6th Floor, Gyeonggi R&DB Center, 906-5 Iui-dong, Yeongtong-gu,
Suwon-si, Gyeonggi-do, 443-766, Korea
Tel : 82-31-888-5300, FAX : 82-31-888-5398

Table of Contents

List of Figures

List of Tables

Introduction

PI4008K is FHD ISP(Image Signal Processor) with a multi-standard Analog HD transmitter. Key features of PI4008K are listed below.

- Image Input
  - Input Resolution
    - 1920x1080p @ 25/30
  - Bayer Interface
    - 10bit data @ maximum 74.25MHz
- Image Output
  - Analog HD : PVI Tx
    - Up to 1920x1080p @ 25/30
    - Video DAC with 10bit @ maximum 148.5MHz, including UTC
- CPU Platform
  - 32bit CPU
  - UART
  - Timer/PWM
  - WDT
  - SPI
  - Single/Dual SPI
  - I2CM/I2CS
  - GPIO
  - DMA
- ISP
  - details in ISP chapter
- OSD
  - Font Layer
  - RLE Layer
  - Private Zone Mask
- Analog Blocks

  - PLL, 27MHz to 297/148.5/74.25MHz
  - ADC, low sample rate
  - UTC comparator
  - Video DAC
- Operation temperature
  - -30 ~ 85[°C] @ ambient
- Package
  - QFN68

Figure 1 shows the functional block diagram of PI4008K. SDC can be optionally enabled under Firmware control.

BT digital output is available only on QFN68 package and QFN48 only supports Analog Output.

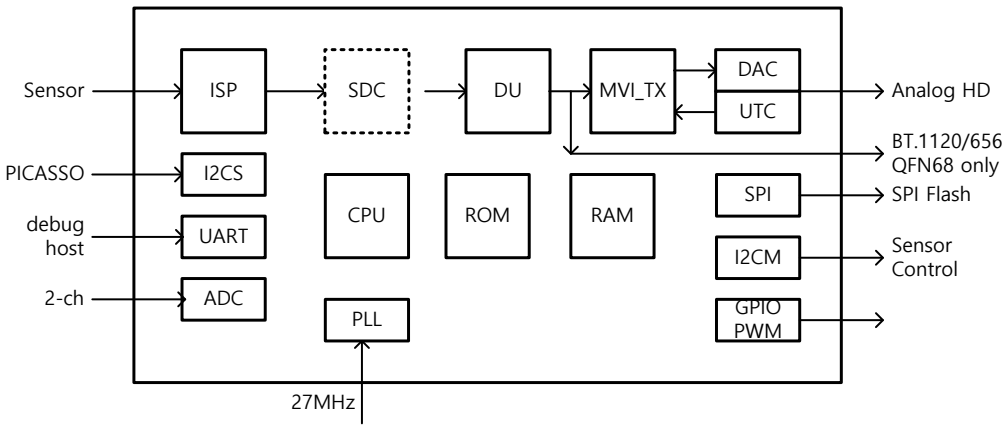

Figure 1 TOP Block Diagram

Pin Description

Figure 2 shows the pin configuration of PI4008K.

Table 1 describes each pins.

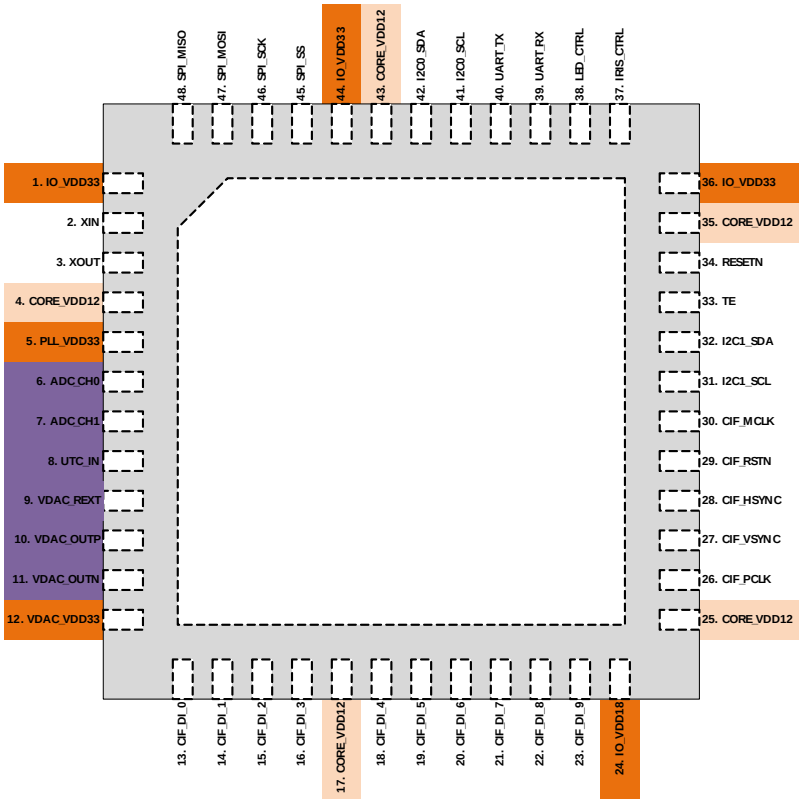

Figure 2 PI4008K Package View

Table 1 Register Table - PIN Description

pin	name	power domain	description
1	IO_VDD33		IO VDD for 3.3V
2	XIN	IO_VDD33	Crystal Oscillator Input
3	XOUT		Crystal Oscillator Output
4	CORE_VDD12		Core VDD for 1.25V
5	PLL_AVDD33		PLL Analog VDD for 3.3V
6	ADC_CH0	VDAC_VDD33	Analog to Digital Converter Channel 0
7	ADC_CH1		Analog to Digital Converter Channel 1
8	UTC_IN		Analog input for the Up the Coax channel
9	VDAC_REXT		External Reference Input for the Video Digital to Analog Converter
10	VDAC_OUTP		Positive Analog Output for the Video Digital to Analog Converter
11	VDAC_OUTN		Negative Analog Output for the Video Digital to Analog Converter
12	VDAC_VDD33		Video DAC VDD for 3.3V

13	CIF_DI_0	IO_VDD18	Parallel Data Input for the Camera Interface
14	CIF_DI_1		Parallel Data Input for the Camera Interface
15	CIF_DI_2		Parallel Data Input for the Camera Interface
16	CIF_DI_3		Parallel Data Input for the Camera Interface
17	CORE_VDD12		Core VDD for 1.25V
18	CIF_DI_4	IO_VDD18	Parallel Data Input for the Camera Interface
19	CIF_DI_5		Parallel Data Input for the Camera Interface
20	CIF_DI_6		Parallel Data Input for the Camera Interface
21	CIF_DI_7		Parallel Data Input for the Camera Interface
22	CIF_DI_8		Parallel Data Input for the Camera Interface
23	CIF_DI_9		Parallel Data Input for the Camera Interface
24	IO_VDD18		IO VDD for 1.8V
25	CORE_VDD12		Core VDD for 1.25V
26	CIF_PCLK	IO_VDD18	Pixel Clock Input for the Camera Interface
27	CIF_VSYNC		Vertical Sync Input for the Camera Interface
28	CIF_HSYNC		Horizontal Sync Input for the Camera Interface
29	CIF_RSTN		Reset Output for the Camera Interface
30	CIF_MCLK		Master Clock Output for the Camera Interface
31	I2C1_SCL		I2C Serial Clock for sensor control
32	I2C1_SDA		I2C Serial Data for sensor control
33	TE	IO_VDD33	Test Enable Input
34	RESETN		Chip Reset Input
35	CORE_VDD12		Core VDD for 1.25V
36	IO_VDD33		IO VDD for 3.3V
37	IRIS_CTRL	IO_VDD33	IRIS control output
38	LED_CTRL		IR LED control output
39	UART_RX		UART RX input
40	UART_TX		UART TX output
41	I2C0_SCL		I2C Serial Clock for the Picasso tune
42	I2C0_SDA		I2C Serial Data for the Picasso tune
43	CORE_VDD12		Core VDD for 1.25V
44	IO_VDD33		IO VDD for 3.3V
45	SPI_SS	IO_VDD33	SPI Slave Select Output
46	SPI_SCK		SPI Serial Clock Output
47	SPI_MOSI		SPI Master Output Slave Input
48	SPI_MISO		SPI Master Input Slave Output
	Thermal PAD		Global Ground

Electrical Characteristics

PI4008K supports ambient operating temperature from -30 ~ 85°C.

DC Characteristics

Table 2 DC Characteristics

Symbol	Description	Min	Typ	Max	Unit
IO_VDD33	I/O VDD for 3.3V	2.97	3.30	3.63	V
VDAC_VDD33	Video DAC VDD for 3.3V	2.97	3.30	3.63	V
PLL_AVDD33	PLL Analog VDD for 3.3V	2.97	3.30	3.63	V
IO_VDD18	Sensor IO VDD for 1.8V~3.3V	1.62	1.80	1.98	V
	Sensor IO VDD for 1.8V~3.3V	2.97	3.30	3.63	V
CORE_VDD12	Core VDD for 1.25V	1.20	1.25	1.30	V

IO_VDD18 is for Sensor interface, it supports both 1.8V and 3.3V supply.

Table 3 Power Consumption

Symbol	Description	Min	Typ	Max	Unit
Current (25FPS)	IO_VDD33		2.59		mA
	VDAC_VDD33 & PLL_AVDD33		5.00		mA
	IO_VDD18		1.55		mA
	CORE_VDD12		87.00		mA
Power (25FPS)	IO_VDD33		8.53		mW
	VDAC_VDD33 & PLL_AVDD33		16.50		mW
	IO_VDD18		2.79		mW
	CORE_VDD12		108.75		mW
Power Total (25FPS)	Sum of all Power		132.22		mW

AC Characteristics

Table 4 AC Characteristics

Symbol	Description	Min	Typ	Max	Unit
Fxin	XIN frequency		27.00		MHz
Fsclk	SPI_SCLK frequency			74.25	MHz
Fsclk	I2C SCL frequency			400.00	KHz
Fpclk	CIF_PCLK frequency			74.25	MHz

Power Sequence

When IO_VDD18 is supplied with 3.3V, the power up sequence is as follows.

```
1. IO_VDD33, VDAC_VDD33, PLL_AVDD33, IO_VDD18
2. CORE_VDD12
```

When IO_VDD18 is supplied with 1.8V, the power up sequence is as follows.

```
1. IO_VDD33, VDAC_VDD33, PLL_AVDD33
2. IO_VDD18
3. CORE_VDD12
```

The power down sequence is the opposite of the power up sequence.

MCU Functional Description

PI4008K includes a 32 Bit RISC Micro-Controller Unit(MCU). MCU is functionally compatible with ARM ISA v2, MCU have 16KByte Mask-ROM and 64KByte On-chip SRAM.

MCU Peripherals

- UART
  - Programmable Baud rate
  - Separated Transmit and receive FIFO
- INTC
  - 32 Interrupt Source
  - Level and Edge Interrupt
  - Programmable Interrupt Priority
- I2C
  - Master only
  - Software programmable clock frequency
  - Bus busy detection
  - Special I2C Slave for ISP Turning
- SPI
  - Memory Mapped SPI Flash Controller
  - General SPI Master and Slave Interface
  - Programmable Clock rate
- ADC
  - 8 bit ADC

ISP(Image Signal Processing)

ISP in PI4008K enhances image quality of input images from the pixel sensor. Supported functions in PI4008K are as follows:

- "Test Pattern (TP) Control"
- "Lens Shading Compensation (LSC)"
- "White Balance Gain"
- "Edge Enhancement"
- "Color Correction (CCR)"
- "RGB Gamma"
- "Y Gamma"
- "De-color"
- "Contrast"
- "Y Offset"
- "Color Saturation"

Test Pattern (TP) Control

TP control generates test images from ISP block. Test images type can be selected by setting tp_control_0 registers. In case of test image types from 0x15 to 0x1A values for tp_control_0, tp_control_1/2/3/4/5 registers are used as color values and the following rule shows how the color value is determined:

- R : {tp_control_1, tp_control_5[7:6]}
- Gr : {tp_control_2, tp_control_5[5:4]}
- Gb : {tp_control_3, tp_control_5[3:2]}
- B : {tp_control_4, tp_control_5[1:0]}

Table 5 shows registers relevant to Test Pattern Control

Table 5 Register Table - Test pattern control

Register name	Address	Bits	Init. Val.	Type	Update	Description
tp_control_0	0x0DC0	[7:0]	0x0000	RW		test image selection
tp_control_1	0x0DC4	[7:0]	0x0000	RW		R[9:2] value for test image
tp_control_2	0x0DC8	[7:0]	0x0000	RW		Gr[9:2] value for test image
tp_control_3	0x0DCC	[7:0]	0x0000	RW		Gb[9:2] value for test image
tp_control_4	0x0DD0	[7:0]	0x0000	RW		B[9:2] value for test image
tp_control_5	0x0DD4	[7:0]	0x0000	RW		{R[1:0], G1[1:0], G2[1:0], B[1:0]} value for test image

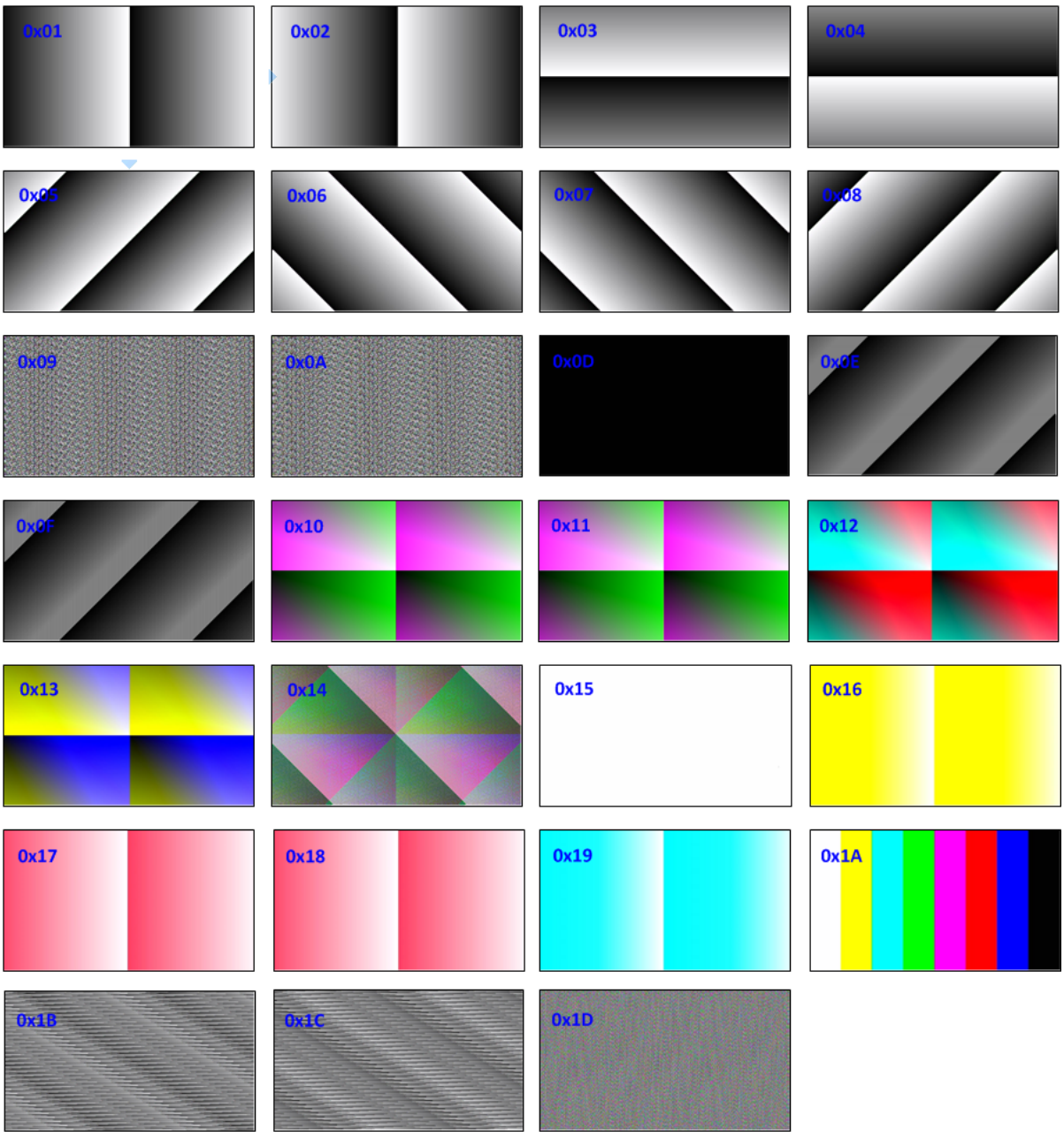

Figure 3 Test image

Lens Shading Compensation (LSC)

Pixel sensor residing in edge of the lens receives less light, whereas ample light exposure is obtained in center pixels. LSC feature compensates this uneven distribution of light exposure. By setting lens_en = 1'b1, LSC feature is enabled. LSC function control components are LSC center, LSC scale, and LSC gain.

- LSC center
  By setting lens_x and lens_y, LSC center is adjusted as shown in Figure 4. This parameter is adjusted if the center of the image is not lined up with the center of the lens.

- LSC scale
  By setting lens_scale, scale rate of lens gain from the LSC center is adjusted. lens_scale value is directly proportional to lens gain value.

- LSC gain
  Lens gain of R, G1, G2, B channel can be separately adjusted through lens_gainr, lens_gain_g1, lens_gain_g2, and lens_gainb registers respectively. Setting high value to the registers result in high lens gain.

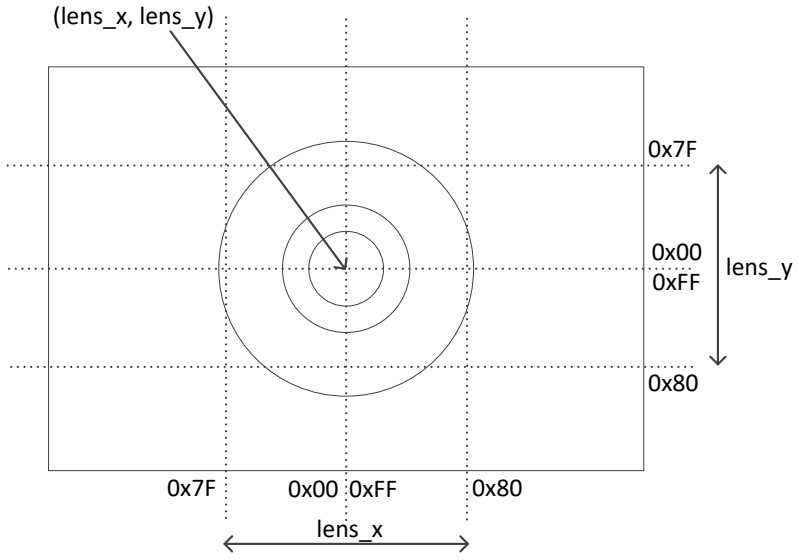

Figure 4 LSC center control

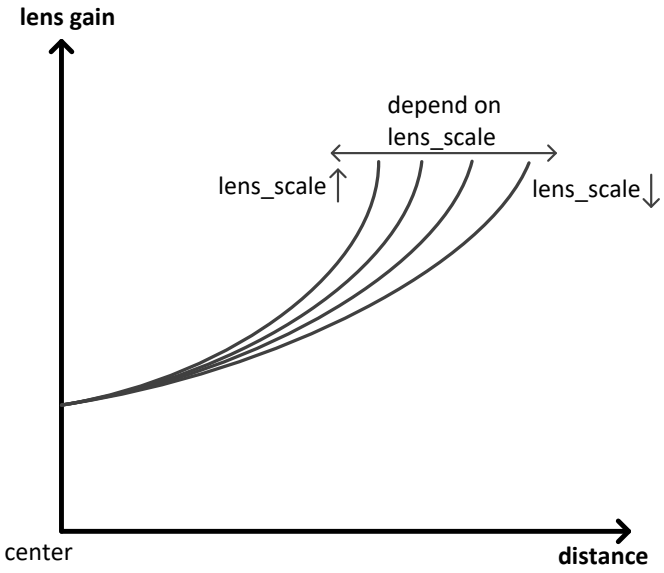

Figure 5 LSC gain fitting with LSC center and LSC scale

Table 6 shows registers relevant to LSC functions.

Table 6 Register Table - LSC

Register name	Address	Bits	Init. Val.	Type	Update	Description
lens_en	0x0D98	[7]	1'b1	RW	aev	Lens shading compensation enable 1'b0 : disable 1'b1 : enable
lens_scale	0x0E0C	[7:0]	0x0051	RW		Lens shading scale control
lens_x	0x0E10	[7:0]	0x0000	RW		Lens shading center control
lens_y	0x0E14	[7:0]	0x0000	RW		
lens_gainr	0x0E18	[7:0]	0x0000	RW	aev	R gain for lens shading
lens_gaing1	0x0E1C	[7:0]	0x0000	RW	aev	G1 gain for lens shading
lens_gaing2	0x0E20	[7:0]	0x0000	RW	aev	G2 gain for lens shading
lens_gainb	0x0E24	[7:0]	0x0000	RW	aev	B gain for lens shading

White Balance Gain

WB gain is applied to images to remove the unrealistic color coming from different color temperature. Proper application of WB results in objects which appear white in person are displayed white in the output image. PI4008K includes two modes of WB process: automatic WB mode and manual WB mode. Automatic WB mode and manual WB mode are selected by setting wb_manual = 1'b0 and wb_manual = 1'b1 respectively. In automatic WB mode, ISP firmware attempts to evaluate proper WB gain and stores to wb_r/g/bgain registers. Whereas, in manual WB mode, users apply desired WB gain by writing values to wb_mr/mg/mbgain.

Table 7 shows registers relevant to WB gain

Table 7 Register Table - White balance gain

Register name	Address	Bits	Init. Val.	Type	Update	Description
wb_rgain_h	0x0E3C	[7:0]	0x0000	RW	aev	Auto WB gain
wb_rgain_l	0x0E40	[7:0]	0x005D	RW	aev	
wb_ggain_h	0x0E44	[7:0]	0x0000	RW	aev	
wb_ggain_l	0x0E48	[7:0]	0x0040	RW	aev	
wb_bgain_h	0x0E4C	[7:0]	0x0000	RW	aev	
wb_bgain_l	0x0E50	[7:0]	0x005E	RW	aev	
wb_mrgain_h	0x0E58	[7:0]	0x0000	RW	aev	Manual WB gain
wb_mrgain_l	0x0E5C	[7:0]	0x005D	RW	aev	
wb_mggain_h	0x0E60	[7:0]	0x0000	RW	aev	
wb_mggain_l	0x0E64	[7:0]	0x0040	RW	aev	
wb_mbgain_h	0x0E68	[7:0]	0x0000	RW	aev	
wb_mbgain_l	0x0E6C	[7:0]	0x005E	RW	aev	
wb_manual	0x0E70	[0]	0x0000	RW		WB gain mode selection 1'b0 : auto WB gain 1'b1 : manual WB gain

Noise Reduction (NR)

Two modes of NR are supported in PI4008K
NR1 mode is enabled by setting NR1_en = 1'b1. The effectiveness of noise reduction of NR1 mode is adjusted by changing dark_NR1_suppress and dark_NR1_enhance registers. Lower value of dark_NR1_suppress results in higher noise reduction strength. On the other hand, higher value of dark_NR1_enhance results in higher noise reduction strength.
NR2 mode is enabled by setting NR2_en = 1'b1. The effectiveness of noise reduction of NR2 mode is adjusted by changing dark_NR2_suppress. Higher value of dark_NR2_suppress results in lower noise reduction strength. In addition, maximum noise reduction strength is applied when NR2_suppress_en = 1'b0 regardless of dark_NR2_suppress value.

Table 8 shows registers relevant to NR functions.

Table 8 Register Table - NR

Register name	Address	Bits	Init. Val.	Type	Update	Description
NR1_en	0x0E78	[7]	1'b0	RW		NR1 enable 1'b0 : disable 1'b1 : enable
dark_NR1_suppress	0x0E88	[7:0]	0x00FF	RW	aev	Control factor for NR1 effect (Max. : 0xFF)
dark_NR1_enhance	0x0E8C	[7:0]	0x0000	RW	aev	
NR2_en	0x1410	[7]	1'b0	RW	aev	NR2 enable 1'b0 : off 1'b1 : on
NR2_suppress_en	0x1410	[4]	1'b0	RW	aev	Enable for NR2 effect control 1'b0 : off 1'b1 : on
dark_NR2_suppress	0x0E78	[7]	1'b0	RW		Control factor for NR2 effect (Max. : 0x0A)

Edge Enhancement

Edge enhancement function controls the sharpness of input image. The function is enabled by setting edge_en = 1'b1. Control factors for edge enhancement are edge gain, edge threshold, and edge maximum value.

- Edge gain
  Edge is intensified directly by setting high edge gain values. edge_pgain and edge_mgain affects positive edge gain and negative edge gain respectively.

- Edge threshold
  Threshold can be set to exclude edge with certain level to be excluded from edge enhancement process. Edge value smaller than edge_pth are excluded from the process for positive edge. In similar fashion, edge value smaller than edge_mth are excluded from the process for negative edge.

- Edge Max. value
  After edge threshold evaluation, maximum value clamping is proceeded. Maximum edge value for positive edge is dark_ec_pmax and for negative edge is dark_ec_mmax.

Table 9 shows registers relevant to edge enhancement functions.

Table 9 Register Table - Edge enhancement

Register name	Address	Bits	Init. Val.	Type	Update	Description
edge_en	0x0D9C	[3]	1'b1	RW	aev	Edge enhancement enable 1'b0 : disable 1'b1 : enable
edge_pgain	0x0F78	[7:0]	0x0010	RW	aev	Positive edge gain
edge_mgain	0x0F7C	[7:0]	0x0020	RW	aev	Negative edge gain
dark_ec_pmax	0x0F88	[7:0]	0x0080	RW	aev	Positive edge Max. value
dark_ec_mmax	0x0F8C	[7:0]	0x0080	RW	aev	Negative edge Max. value
dark_ec_pth	0x0F80	[7:0]	0x0010	RW	aev	Positive edge threshold
dark_ec_mth	0x0F84	[7:0]	0x0010	RW	aev	Negative edge threshold

Color Correction (CCR)

CCR function utilizes 3 by 3 matrix multiplication to correct RGB color. dark_ccr register reduces the effectiveness of CCR. As dark_ccr value increases, degree of CCR decreases.

$$\begin{bmatrix} R` \\ G` \\ B` \end{bmatrix} = \begin{bmatrix} ccr\_m11 & ccr\_m12 & ccr\_m13 \\ ccr\_m21 & ccr\_m22 & ccr\_m23 \\ ccr\_m31 & ccr\_m32 & ccr\_m33 \end{bmatrix} X \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Figure 6 CCR matrix

Table 10 shows registers relevant to CCR functions.

Table 10 Register Table - CCR

Register name	Address	Bits	Init. Val.	Type	Update	Description
ccr_en	0x0D98	[1]	1'b1	RW	aev	Color correction enable 1'b0 : disable 1'b1 : enable
ccr_m11	0x10C4	[7:0]	0x0031	RW	aev	Color correction matrix value
ccr_m12	0x10C8	[7:0]	0x0085	RW	aev	
ccr_m13	0x10CC	[7:0]	0x008C	RW	aev	
ccr_m21	0x10D0	[7:0]	0x008C	RW	aev	
ccr_m22	0x10D4	[7:0]	0x0042	RW	aev	
ccr_m23	0x10D8	[7:0]	0x0092	RW	aev	
ccr_m31	0x10DC	[7:0]	0x0085	RW	aev	
ccr_m32	0x10E0	[7:0]	0x008E	RW	aev	
ccr_m33	0x10E4	[7:0]	0x0033	RW	aev	
dark_ccr	0x10E8	[7:0]	0x0000	RW	aev	Darkness value for color correction

RGB Gamma

RGB gamma function performs non-linear operation on RGB color after CCR. RGB gamma function can configure two different gamma reference curves: gamma curve1 and gamma curve2. Depending on the dark_rgb_gm setting level, the system determines which curve to apply for RGB (refer to Figure 7). RGB gamma is enabled by setting rgbgm_en = 1'b1.

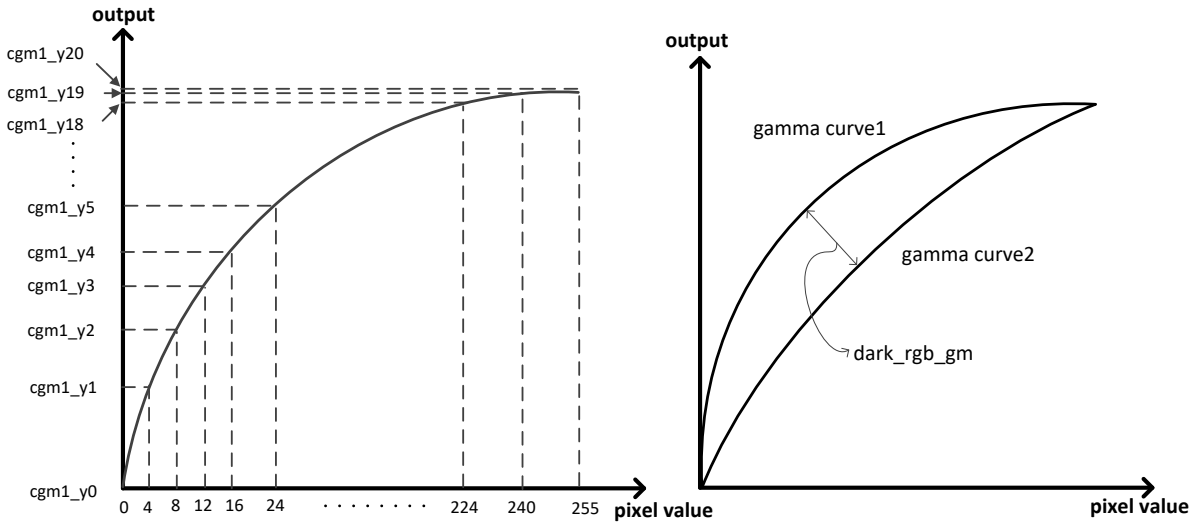

Figure 7 Gamma curve fitting of RGB gamma

Table 11 shows registers relevant to RGB gamma functions.

Table 11 Register Table - RGB gamma

Register name	Address	Bits	Init. Val.	Type	Update	Description
rgbgm_en	0x0D9C	[7]	1'b1	RW	aev	RGB gamma enable 1'b0 : disable 1'b1 : enable
cgm1_y0	0x10F0	[7:0]	0x0000	RW		Gamma curve reference1 for RGB gamma
cgm1_y1	0x10F4	[7:0]	0x0003	RW		
cgm1_y2	0x10F8	[7:0]	0x000E	RW		
cgm1_y3	0x10FC	[7:0]	0x001D	RW		
cgm1_y4	0x1100	[7:0]	0x002C	RW		
cgm1_y5	0x1104	[7:0]	0x0047	RW		
cgm1_y6	0x1108	[7:0]	0x005B	RW		
cgm1_y7	0x110C	[7:0]	0x0077	RW		
cgm1_y8	0x1110	[7:0]	0x008B	RW		
cgm1_y9	0x1114	[7:0]	0x009A	RW		
cgm1_y10	0x1118	[7:0]	0x00A9	RW		
cgm1_y11	0x111C	[7:0]	0x00B5	RW		

Register name	Address	Bits	Init. Val.	Type	Update	Description
cgm1_y12	0x1120	[7:0]	0x00C0	RW		
cgm1_y13	0x1124	[7:0]	0x00C9	RW		
cgm1_y14	0x1128	[7:0]	0x00D2	RW		
cgm1_y15	0x112C	[7:0]	0x00DB	RW		
cgm1_y16	0x1130	[7:0]	0x00E3	RW		
cgm1_y17	0x1134	[7:0]	0x00EB	RW		
cgm1_y18	0x1138	[7:0]	0x00F2	RW		
cgm1_y19	0x113C	[7:0]	0x00F9	RW		
cgm1_y20	0x1140	[7:0]	0x00FF	RW		
cgm2_y0	0x1144	[7:0]	0x0000	RW		
cgm2_y1	0x1148	[7:0]	0x0011	RW		
cgm2_y2	0x114C	[7:0]	0x001B	RW		
cgm2_y3	0x1150	[7:0]	0x0023	RW		
cgm2_y4	0x1154	[7:0]	0x002A	RW		
cgm2_y5	0x1158	[7:0]	0x0037	RW		
cgm2_y6	0x115C	[7:0]	0x0042	RW		
cgm2_y7	0x1160	[7:0]	0x0056	RW		
cgm2_y8	0x1164	[7:0]	0x0068	RW		
cgm2_y9	0x1168	[7:0]	0x0078	RW		
cgm2_y10	0x116C	[7:0]	0x0087	RW		Gamma curve reference2 for RGB gamma
cgm2_y11	0x1170	[7:0]	0x0095	RW		
cgm2_y12	0x1174	[7:0]	0x00A3	RW		
cgm2_y13	0x1178	[7:0]	0x00B0	RW		
cgm2_y14	0x117C	[7:0]	0x00BC	RW		
cgm2_y15	0x1180	[7:0]	0x00C8	RW		
cgm2_y16	0x1184	[7:0]	0x00D4	RW		
cgm2_y17	0x1188	[7:0]	0x00DF	RW		
cgm2_y18	0x118C	[7:0]	0x00EA	RW		
cgm2_y19	0x1190	[7:0]	0x00F5	RW		
cgm2_y20	0x1194	[7:0]	0x00FF	RW		
dark_rgb_gm	0x1198	[7:0]	0x0000	RW	aev	Darkness value for RGB gamma

Y Gamma

Y gamma function performs non-linear operation on Y component. Y gamma function can configure two different gamma reference curves: gamma curve1 and gamma curve2. Depending on the dark_y_gm setting level, the system determines which curve to apply for Y (refer to Figure 8). Y gamma is enabled by setting ygm_en = 1'b1.

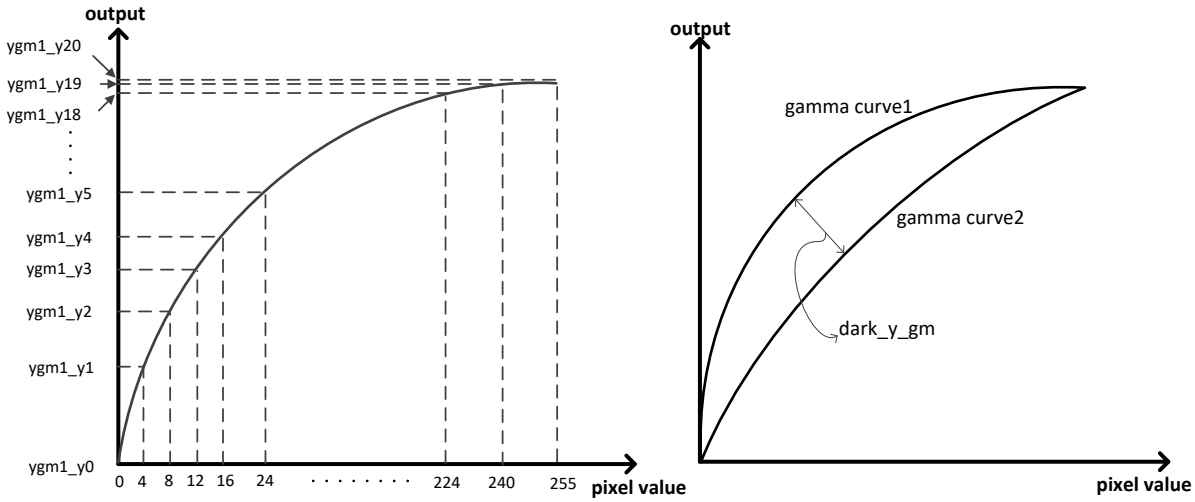

Figure 8 Gamma curve fitting of Y gamma

Table 12 shows registers relevant to Y gamma functions.

Table 12 Register Table - Y Gamma

Register name	Address	Bits	Init. Val.	Type	Update	Description
ygm_en	0x0D9C	[6]	1'b1	RW	aev	Y gamma enable 1'b0 : disable 1'b1 : enable
ygm1_y0	0x1010	[7:0]	0x0000	RW		Gamma curve reference1 for Y gamma
ygm1_y1	0x1014	[7:0]	0x000F	RW		
ygm1_y2	0x1018	[7:0]	0x0026	RW		
ygm1_y3	0x101C	[7:0]	0x0037	RW		
ygm1_y4	0x1020	[7:0]	0x0043	RW		
ygm1_y5	0x1024	[7:0]	0x0054	RW		
ygm1_y6	0x1028	[7:0]	0x0062	RW		
ygm1_y7	0x102C	[7:0]	0x0077	RW		
ygm1_y8	0x1030	[7:0]	0x0088	RW		
ygm1_y9	0x1034	[7:0]	0x0096	RW		
ygm1_y10	0x1038	[7:0]	0x00A4	RW		
ygm1_y11	0x103C	[7:0]	0x00B0	RW		

Register name	Address	Bits	Init. Val.	Type	Update	Description
ygm1_y12	0x1040	[7:0]	0x00BB	RW		
ygm1_y13	0x1044	[7:0]	0x00BE	RW		
ygm1_y14	0x1048	[7:0]	0x00CF	RW		
ygm1_y15	0x104C	[7:0]	0x00D8	RW		
ygm1_y16	0x1050	[7:0]	0x00E0	RW		
ygm1_y17	0x1054	[7:0]	0x00E9	RW		
ygm1_y18	0x1058	[7:0]	0x00F1	RW		
ygm1_y19	0x105C	[7:0]	0x00F8	RW		
ygm1_y20	0x1060	[7:0]	0x00FF	RW		
ygm2_y0	0x1064	[7:0]	0x0000	RW		
ygm2_y1	0x1068	[7:0]	0x001A	RW		
ygm2_y2	0x106C	[7:0]	0x0026	RW		
ygm2_y3	0x1070	[7:0]	0x002F	RW		
ygm2_y4	0x1074	[7:0]	0x0038	RW		
ygm2_y5	0x1078	[7:0]	0x0046	RW		
ygm2_y6	0x107C	[7:0]	0x0051	RW		
ygm2_y7	0x1080	[7:0]	0x0066	RW		
ygm2_y8	0x1084	[7:0]	0x0077	RW		
ygm2_y9	0x1088	[7:0]	0x0086	RW		
ygm2_y10	0x108C	[7:0]	0x0095	RW		Gamma curve reference2 for Y gamma
ygm2_y11	0x1090	[7:0]	0x00A2	RW		
ygm2_y12	0x1094	[7:0]	0x00AF	RW		
ygm2_y13	0x1098	[7:0]	0x00BA	RW		
ygm2_y14	0x109C	[7:0]	0x00C5	RW		
ygm2_y15	0x10A0	[7:0]	0x00D0	RW		
ygm2_y16	0x10A4	[7:0]	0x00DA	RW		
ygm2_y17	0x10A8	[7:0]	0x00E4	RW		
ygm2_y18	0x10AC	[7:0]	0x00ED	RW		
ygm2_y19	0x10B0	[7:0]	0x00F6	RW		
ygm2_y20	0x10B4	[7:0]	0x00FF	RW		
dark_y_gm	0x10B8	[7:0]	0x0000	RW	aev	Darkness value for Y gamma

De-color

De-color function reduces chroma level and is enabled by setting dc_en = 1’b1. High dark_dc level results in achromatic color. The maximum value of dark_dc is 0x3F.

Table 13 shows registers relevant to decolor functions.

Table 13 Register Table - De-color

Register name	Address	Bits	Init. Val.	Type	Update	Description
dc_en	0x0DB0	[2]	1'b0	RW	aev	De-color enable 1'b0 : disable 1'b1 : enable
dark_dc	0x11AC	[7:0]	0x0000	RW	aev	De-color factor

Contrast

Contrast function performs linear operation on Y component. y_cont_th2 acts as the reference point of linear function, and y_cont_slope2 determines the linear function’s slope.

Table 14 Register Table - Contrast

Register name	Address	Bits	Init. Val.	Type	Update	Description
y_cont_th2	0x11CC	[7:0]	0x0080	RW	aev	X-axis standard for contrast line
y_cont_slope2	0x11D0	[7:0]	0x0040	RW	aev	Slope for contrast line

Y Offset

Y offset is the brightness offset of the system. The number representation of Y offset is 2’s complement. Y offset level can be adjusted by changing ybrightness register.

Table 15 shows registers relevant to Y offset functions.

Table 15 Register Table - Y offset

Register name	Address	Bits	Init. Val.	Type	Update	Description
ybrightness	0x11C8	[7:0]	0x0000	RW	aev	Y offset value(2's complement)

Color Saturation

Color saturation functions performs 2 by 2 matrix operation on chroma domain (Cb/Cr) to adjust hue and saturation. user_cs register is additional multiplication coefficient parameter for cs11 and cs22 components

$$\begin{bmatrix} Cb` \\ Cr` \end{bmatrix} = \begin{bmatrix} user\_cs \times cs11 & cs12 \\ cs21 & user\_cs \times cs22 \end{bmatrix} \times \begin{bmatrix} Cb \\ Cr \end{bmatrix}$$

Figure 9 Color saturation matrix

Table 16 shows registers relevant to color saturation functions.

Table 16 Register Table - Color saturation

Register name	Address	Bits	Init. Val.	Type	Update	Description
cs11	0x11D8	[7:0]	0x001C	RW	aev	Color saturation matrix value
cs12	0x11DC	[7:0]	0x0004	RW	aev	
cs21	0x11E0	[7:0]	0x008C	RW	aev	
cs22	0x11E4	[7:0]	0x0025	RW	aev	
user_cs	0x11E8	[7:0]	0x0020	RW		User color saturation gain

ISP Windowing

Based on the input image size, windowing can be performed to control the ISP output image size. Figure 10 shows ISP window control corresponding to windowx1/2, windowy1/2 register configuration.

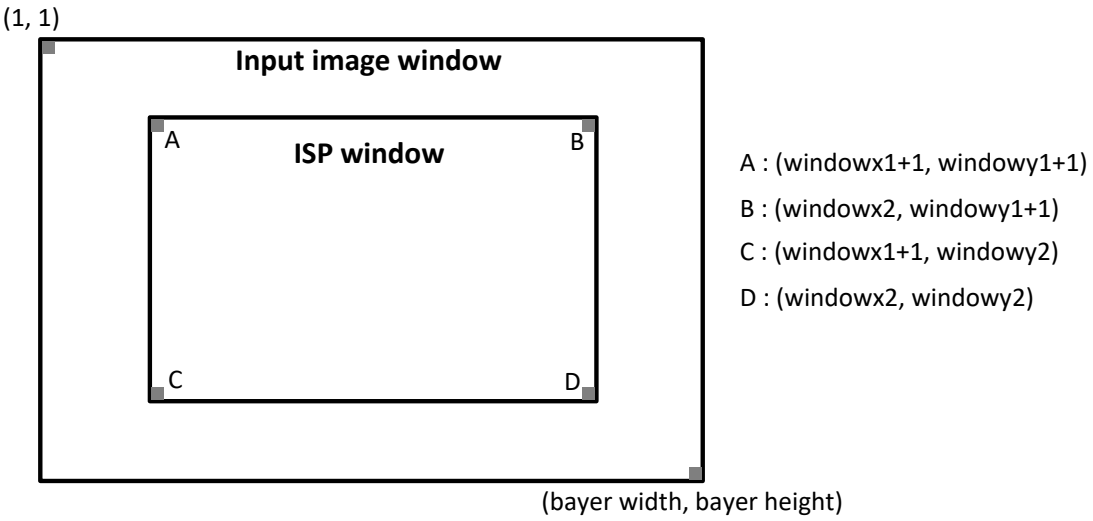

Figure 10 ISP windowing

Table 17 shows registers relevant to ISP windowing.

Table 17 Register Table - ISP window setting

Register name	Address	Bits	Init. Val.	Type	Update	Description
windowx1_h	0x1360	[2:0]	0x0000	RW	aev	ISP window control
windowx1_l	0x1364	[7:0]	0x0008	RW	aev	
windowy1_h	0x1370	[2:0]	0x0000	RW	aev	
windowy1_l	0x1374	[7:0]	0x0008	RW	aev	
windowx2_h	0x1368	[2:0]	0x0007	RW	aev	
windowx2_l	0x136C	[7:0]	0x0088	RW	aev	
windowy2_h	0x1378	[2:0]	0x0004	RW	aev	
windowy2_l	0x137C	[7:0]	0x0040	RW	aev	

Flicker Detection

PI4008K includes flicker detection feature. Generally, operating frequency of light source is either 60 Hz or 50 Hz. Therefore, PI4008K's flicker detection feature is pre-configured states with 60 Hz light source frequency as state A and 50 Hz light source frequency as state B.
Three different flicker detection mode is available in PI4008K: auto mode, manual A mode, and manual B mode.

- Auto mode(fd_en = 1'b1, manual_A = 1'b0, manual_B = 1'b0)
  When flicker in image is detected, current state is toggled. In other word, current state is switched to the other state.
- manual_A mode(fd_en = 1'b0, manual_A = 1'b1, manual_B = 1'b0)
  Manual A mode puts flicker detection state in state A regardless of flicker. Factory setting of PI4008K is configured for 60 Hz light source.
- manual_B mode(fd_en = 1'b0, manual_A = 1'b0, manual_B = 1'b1)
  Manual B mode puts flicker detection state in state B regardless of flicker. Factory setting of PI4008K is configured for 50 Hz light source.

Table 18 shows registers relevant to flicker detection.

Table 18 Register Table - Flicker detection

Register name	Address	Bits	Init. Val.	Type	Update	Description
fd_en	0x0D54	[6]	1'b0	RW		flicker detection enable(auto_mode) 0b : disable 1b : enable
manual_A	0x0D54	[3]	1'b0	RW		manual A mode enable 0b : disable 1b : enable
manual_B	0x0D54	[2]	1'b0	RW		manual B mode enable 0b : disable 1b : enable

Auto Exposure Control

AE Window Setting

AE feature gathers brightness information from 5 different sections of an image. This sections is called AE window and can be controlled by AE-window1/2/3/4/C registers.

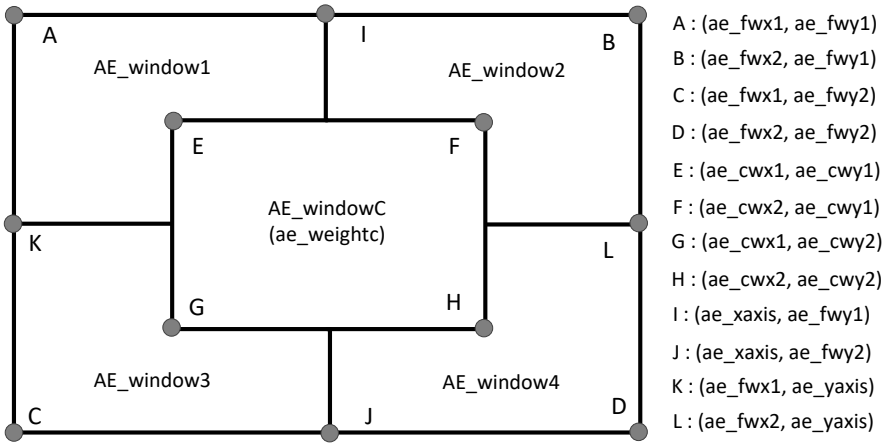

Figure 11 AE window setting

Table 19 shows registers relevant to AE window.

Table 19 Register Table - AE window setting

Register name	Address	Bits	Init. Val.	Type	Update	Description
ae_fwx1_h	0x12B4	[2:0]	0x0000	RW		
ae_fwx1_l	0x12B8	[7:0]	0x0008	RW		
ae_fwx2_h	0x12BC	[2:0]	0x0007	RW		
ae_fwx2_l	0x12C0	[7:0]	0x0088	RW		
ae_fwy1_h	0x12C4	[2:0]	0x0000	RW		
ae_fwy1_l	0x12C8	[7:0]	0x0008	RW		
ae_fwy2_h	0x12CC	[2:0]	0x0004	RW		
ae_fwy2_l	0x12D0	[7:0]	0x0040	RW		
ae_cwx1_h	0x12D4	[2:0]	0x0002	RW		AE window control
ae_cwx1_l	0x12D8	[7:0]	0x0088	RW		
ae_cwx2_h	0x12DC	[2:0]	0x0005	RW		
ae_cwx2_l	0x12E0	[7:0]	0x0008	RW		
ae_cwy1_h	0x12E4	[2:0]	0x0001	RW		
ae_cwy1_l	0x12E8	[7:0]	0x0070	RW		
ae_cwy2_h	0x12EC	[2:0]	0x0002	RW		
ae_cwy2_l	0x12F0	[7:0]	0x00D8	RW		
ae_xaxis_h	0x12F4	[2:0]	0x0003	RW		

Register name	Address	Bits	Init. Val.	Type	Update	Description
ae_xaxis_l	0x12F8	[7:0]	0x00C8	RW		
ae_yaxis_h	0x12FC	[2:0]	0x0002	RW		
ae_yaxis_l	0x1300	[7:0]	0x0024	RW		

Auto White Balance Control

AWB Window Setting

PI4008K can select specific region of an image to perform AWB process. This region is called AWB window and, normally, has the same size as ISP window for optimal operation.

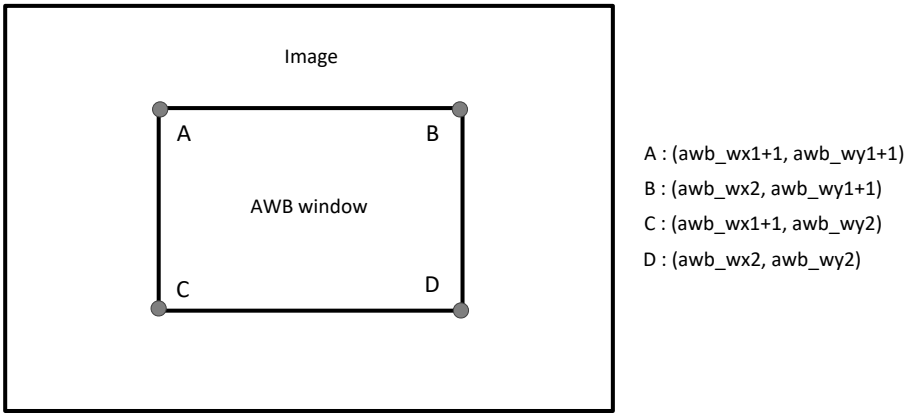

Figure 12 AWB window setting

Table 20 shows registers relevant to AWB window.

Table 20 Register Table - AWB window setting

Register name	Address	Bits	Init. Val.	Type	Update	Description
awb_wx1_h	0x1304	[2:0]	0x0000	RW		AWB window control
awb_wx1_l	0x1308	[7:0]	0x0008	RW		
awb_wx2_h	0x130C	[2:0]	0x0007	RW		
awb_wx2_l	0x1310	[7:0]	0x0088	RW		
awb_wy1_h	0x1314	[2:0]	0x0000	RW		
awb_wy1_l	0x1318	[7:0]	0x0008	RW		
awb_wy2_h	0x131C	[2:0]	0x0004	RW		
awb_wy2_l	0x1320	[7:0]	0x0040	RW		

DU (Display Unit)

DU (Display Unit) covers PZ(Private Zone) Masking, OSD (On Screen Display) for menu, BTO (BT output formatter), PVI-Tx. It also has ATG (Asynchronous Timing Generator) that support low operational clock while supporting standard clock for BT output.

Figure 13 shows the block diagram of DU and the order of functions, PZ masks the input image first, OSD blend text or graphics to the image, BTO formats to send the blended image to the ports for digital or PVI for analog output.

Typical position for ATG is between OSD and BTO, ATG supports low clock for input, standard clock for output. For example, 59.4MHz input clock and 74.25MHz output clock to lower the power consumption of PI4008K ATG also supports synchronous clocks for both input and output.

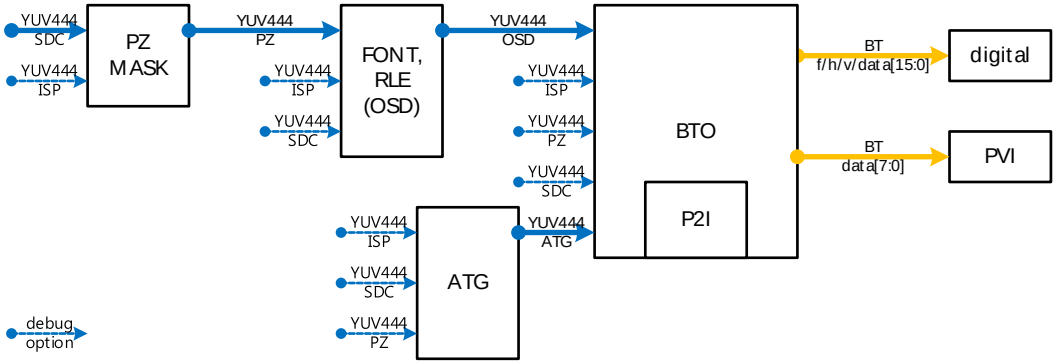

Figure 13 DU Block Diagram

The dotted lines in Figure 13 are for debugging purpose only, typical image flow is from PZ, OSD, (ATG), BTO, PVI-Tx.

OSD includes FONT layer and Graphics Layer, OSD Menu is implemented based on FONT layer. Graphics Layer supports RLE(Run Length Encoding) but it has limited application.

The following table shows the possible combination to lower the core clock frequency.

Table 21 Async TG for FHD case

I/O MHz	Core MHz	Description
74.25	74.25	typical case for 25/30 Hz
74.25	59.4	low core clock case only for 25 Hz

PZ (Private Zone)

PZ block has 8 different area to mask the original image for private reasons, each area can be enabled/disabled independently.

The minimum block size in an area is 8x8 pixels,

the minimum postion steps is also in 8 pixels.

FONT Layer

Figure 14 shows the block diagram for FONT layer.

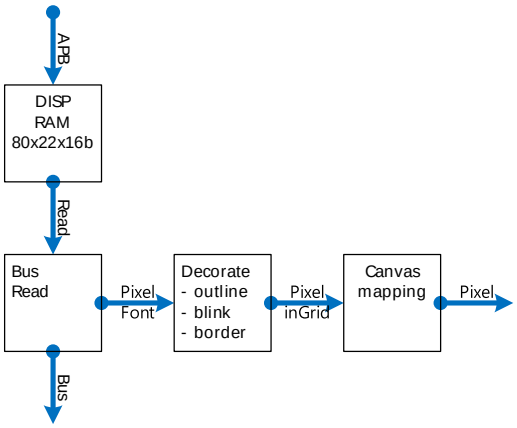

Figure 14 OSD FONT Block Diagram

It has a display RAM that supports maximum 80x22 characters. The actual number of characters displayed on-screen is decided by register settings.

Each characters have 16-bit field to represent a character with attributes as shown in Table 22

Table 22 OSD Font Character and Attributes

Bit	Description
15	B - blink enabled/disabled
14	O - color index of Outline (Border1 and Border2)
13:12	BG - color index of BackGround
11:9	FG - color index of ForeGround
8:0	CH - index to character (FONT)

FONT layer supports maximum 80x22 characters, the display RAM implemented with 1760 x 16bit RAM. Figure 15 The address calculation from X, Y postion of character is as follow.

- Address = X + Y x 80 (fixed)

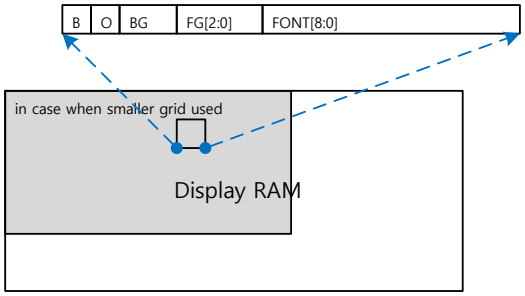

Figure 15 OSD FONT Display RAM

The color registers have Alpha/Red/Green/Bule fields, however a global alpha value can also be applied by (osd_font_alpha) register. When global alpha is enabled, the alpha field for each pixel is ignored.

FONT Layer is generating on-screen image based on RGB color register value, and it supports RGB2YUV conversion for YUV based mixers. When YUV based on-screen FONT is applied RGB2YUV for FONT layer can be set to bypass without doing color space conversion.

RLE Layer

RLE layer has 4 area which can draw 4 different image on-screen, RLE layer supports both Run-Length-Encoded pixel and raw image pixel, each pixel is an index to LUT that holds 256 different color with Alpha/Red/Green/Blue.

Figure 16 shows the functional block diagram in RLE layer. 4 independent area can be controlled, Each area can be overlapped or move out side of visible area, but it's recomended that the amount be minimum.

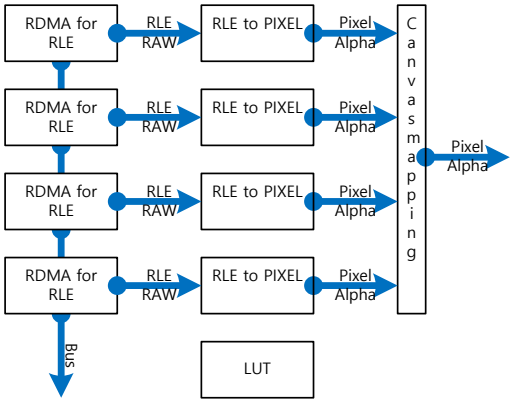

Figure 16 OSD RLE Block Diagram

RLE Layer is generating on-screen image based on RGB color domain, and it supports RGB2YUV conversion for YUV based mixers, When YUV based on-screen image is applied RGB2YUV for RLE layer can be set to bypass without doing color space conversion.

RGB2YUV conversion

RGB2YUV color converters in FONT layer and RLE layer have an identical architecture with independent set of parameters for color conversion. The following equation applied to calculate R/G/B from Y/U/V.

```
Y = (R x ycoef0 + G x ycoef1 + B x ycoef2 + ycoef3) / 512
U = (R x ucoef0 + G x ucoef1 + B x ucoef2 + ucoef3) / 512
V = (R x vcoef0 + G x vcoef1 + B x vcoef2 + vcoef3) / 512
```

coef0/coef1/coef2 are in signed 12.9F format that has 1 sign bit, 2 integer bits, 9 fractional bits.

coef3 is in signed 20.17F format that has 1 sign bit, 2 integer bits, 17 fractional bits.

To remove the fractional part after the matrix operation, 9 bits are truncated from the result before getting Y/U/V values.

BTO (BT Output Formatter)

Registers in BTO are mainly controlled by F/W, it's not recomended to change the value during operation.

BTO base address is 0xf090_0000.

Table 23 Register Table : BTO Control

Register name	Address	Bits	Init. Val.	Type	Description
	Hex				
bto_ctrl0	0400	[31:0]	0x0000_0000	RW	[7] vav_also_use_hav_rise, for debugging only 1: VAV must be in synchronous to HAV fall by BT standard, but this option makes VAV also be in synchronous to HAV rise and fall. [6] sd_outfmt_md 1: SD mode, 0: HD mode [5] sd_960h_md 1: SD 960H mode, 0: SD 720H mode [4] sd_fld_pol 1: field sync (FAV, FSYNC) inversion [3] outfmt_16bit 1: 16-bit data mode, 0: 8-bit data mode [2] outfmt_bt656 1: BT.656 mode, 0: BT.1120 mode [1] outfmt_yc_inv 1: swap Y/C [0] bt1120_limit_digital 1: data limited to 16-240, 0: data limited to 1-254
bto_ctrl1	0404	[31:0]	0x0000_0000	RW	[7] bto_clk_pol 1: BTO clock inversion [6:4] bto_vsync_delay, for debug purpose only 1~7: VSYNC edge shifted right to 1~7 clock 0: VSYNC transition aligned to HSYNC transition
bto_state	0408	[31:0]	0x0000_0000	RO	[5] yuvi_hsync, HSYNC of YUV input to BTO block [4] yuvi_vsync, VSYNC of YUV input to BTO block [2] bto_fsync, FSYNC from BTO block [1] bto_hsync, HSYNC from BTO block [0] bto_vsync, VSYNC from BTO block

PVI Encoder

PVI encoder can convert and output Multi-Standard HD Analog of HD-CVI/HDT/HDA from digital video input. It is supprot to change as PVI video format from H/V Sync data, Luminance, Chrominance of digital video input. In addition, It is supports Bi-Directional Coaxal PTZ interface for transmit and receive HD UTC information.

Color Subcarrier Selection

Color subcarrier of various output format can be control through register of Table 24 as like Table 25 .

Table 24 Register Table - Subcarrier register

Register name	Address	Bits	Init. Val.	Type	Update	Description
FSC_MD_SEL[2:0]	0x0D60	[6:4]	3'b000	RW		Fixed Color Subcarrier Selection
FSC_CLK_SEL[2:0]	0x0D60	[2:0]	3'b000	RW		Color Subcarrier Selection

Table 25 Register Table - Subcarrier selection

FSC_MD_SEL FSC_CLK_SEL	5 (HD-CVI)	6 (HD-HDT)	7 (HD-HDA)
0	720p@60	720p@60	720p@60
1	720p@50	720p@50	720p@50
2	720p@30	720p@30 (Old)	720p@30
3	720p@25	720p@25 (Old)	720p@25
4	1080p@30	1080p@30	1080p@30
5	1080p@25	1080p@25	1080p@25
6	x	720p@30 (New)	x
7	x	720p@25 (New)	x

Video Tunning

Table 26 is register table that related to video image.

Table 26 Register Table - Video tunning

Register name	Address	Bits	Init. Val.	Type	Update	Description
TST_PT_SEL[3:0]	0x0C4C	[7:4]	4'b0000	RW		Selection of Test Pattern 0 : Black, 1 : Blue, 2 : Red, 3 : Magenta, 4 : Green, 5 : Cyan, 6 : Yellow, 7 : White, 8 : Color Bar, 9 : Gray Bar, 10 : Hatch Pattern, 11 : Center Box Pattern, 12 : H Sweep Pattern, 13 : H/V Frequency Sweep Pattern,

Register name	Address	Bits	Init. Val.	Type	Update	Description
						14 : Complex Mixed Pattern0, 15 : Complex Mixed Pattern1
CONT_EN	0x0C4C	[3]	1'b0	RW		Selection Contrast Control Enable 0 : Bypass 1 : Enable
BRT_EN	0x0C4C	[2]	1'b0	RW		Selection Brightness Control Enable 0 : Bypass 1 : Enable
SAT_EN	0x0C4C	[1]	1'b0	RW		Selection Saturation Control Enable 0 : Bypass 1 : Enable
HUE_EN	0x0C4C	[0]	1'b0	RW		Selection Hue Control Enable 0 : Bypass 1 : Enable
CONT	0x0C50	[7:0]	0x80	RW		Contrast Control Value 0 : Minimum ~ 128 : Bypass ~ 255 : Maximum
BRT	0x0C54	[7:0]	0x80	RW		Brightness control value
SAT	0x0C58	[7:0]	0x80	RW		Color saturation control value
HUE	0x0C5C	[7:0]	0x80	RW		Hue control value
Y_GAIN	0x0C70	[7:0]	0x00	RW		Selection Y Amplitude for Output Y = 0.591 x (Y709 – 16), Y_GAIN = 0.591x1024 = 605
U_GAIN	0x0C74	[7:0]	0x00	RW		Selection U Amplitude for Output U = 0.578 x 0.874 (CB – 128), U_GAIN = 517
V_GAIN	0x0C78	[7:0]	0x00	RW		Selection V Amplitude for Output V = 0.578 x 1.230 x (Cr – 128), V_GAIN = 728
CB_OS	0x0D74	[7:0]	8'h80	RW		Selection CB Offset ~ : - CB Offset 8’h80 : Bypass(Default) ~ : + CB Offset
CR_OS	0x0D78	[7:0]	8'h80	RW		Selection CR Offset ~ : - CR Offset 8’h80 : Bypass(Default) ~ : + CR Offset

Revision History

Version	Date [D/M/Y]	Notes	Writer
0.0	03/02/2017	(Preliminary)	Sang Hyun Han
0.1	13/02/2017	Electrical Characteristics, Power Sequence chapter added.	Sang Hyun Han
0.2	14/03/2017	Minor update & add to PVI encoder description	Sang Hyun Han
0.3	26/07/2018	Modify to electrical Characteristics	Sang Hyun Han
0.4	05/10/2018	Delete to SD output and modify to register address of PVI encoder	Sang Hyun Han
0.5	16/11/2018	Delete MIPI Feature	Yeari Seo
0.6	27/02/2019	Modify to introduction	Sanghyun Han