Crystal Image through
Imaging Innovation

PIXELPLUS

Brief Datasheet

1/4" HD class CMOS Image Sensor with HD-Analog Transmitter

PV2109K

Rev 0.0

Last Update : 20. Feb. 2017

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▶ Features

▷ 1296 x 736 Effective pixel array with
RGB bayer color filters and micro-lens.

▷ Output
◆ Digital Output Format
- YUV422 / RGB565 / RGB444 / Bayer
- SMPTE296M

◆ Analog Output Format
- HD-Analog

◆ Output Interface
- 8/10 & 16/20 Bits Digital parallel interface
- HD-Analog

▷ Image processing on chip
lens shading, gamma/defect/color correction
NR (2D noise reduction), color interpolation,
edge enhancement, brightness, contrast
auto black level, auto white balance
auto exposure control
and back light compensation

▷ Selective Color shift

▷ Horizontal / Vertical mirroring

▷ Automatic flicker cancellation

▷ Smart IRLED/TDN controller

▷ 4 overlay function by using SPIROM

▷ I2C/SPI master include

▷ Software Reset

▷ Crystal input support

▷ On-chip Phase Locked Loop(PLL)

▷ CLCC/CSP Package type supports

Pixel Size	3 um x 3 um
Effective Pixel Array	1296 (H) x 736 (V)
Effective Image Area	3.888 mm x 2.208 mm
Optical Format	1/4 inch
Input Clock frequency	27Mhz
Max. Frame Rate	30 fps @ SMPTE296M 30 fps @ YUV 30 fps @ HD-Analog
Dark Signal	3.9 [mV/sec] @ 60℃
Sensitivity	3.5 [V/Lux.sec]
Power Supply	AVDD/CVDD/SVDD/ PLLVDD : 3.3V HVDD : 1.8V ~ 3.3V DVDD : 1.2V
Power Consumption	339 mW @ Dynamic_25fps 355 mW @ Dynamic_30fps
	3.5 mW @ Standby
Operating Temp. (Fully Functional Temp)	-40 ~ 105 [℃]
Dynamic Range	65 [dB]
SNR	44 [dB]

[Table 1] Typical Parameters

▶ Signal Environment

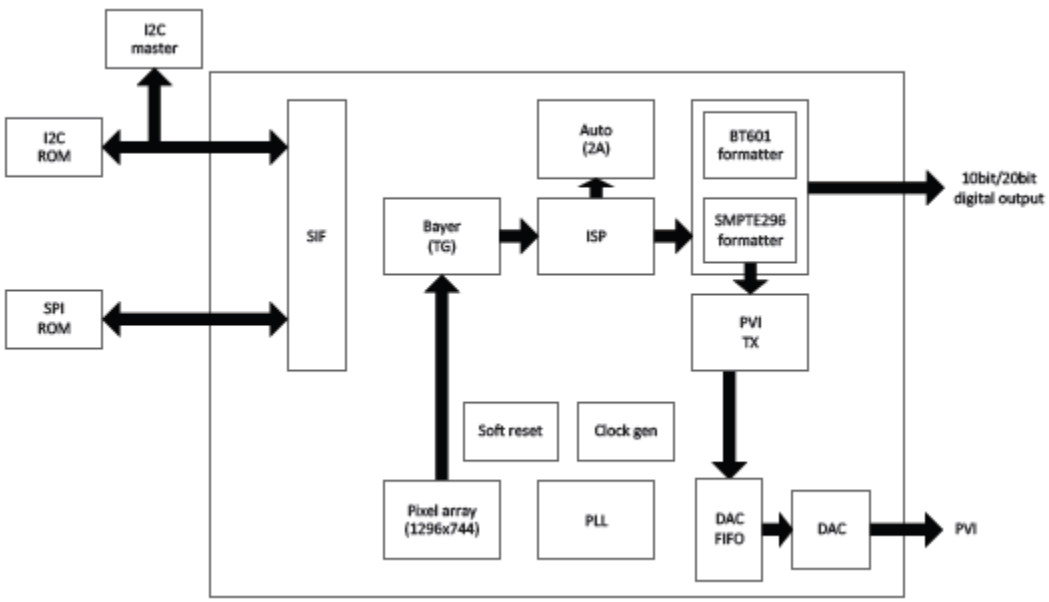
PV2109K don't have tolerant Input pads. The input signal must be equal to HVDD for stable operation. If the power of input signal is higher than recommended, it may flow leakage current by shot circuit path in the input PADs.

▶ Chip Architecture

PV2109K has 1296 x 736 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time processing blocks to produce YCbCr 4:2:2 output data. Image signal processing includes such operations such as gamma correction, contrast stretch, color saturation, white balance, exposure control and back light compensation.

BT601/SMPTE296M formatter supports 10/20-bits digital output and PVI Tx supports PVI (HD-Analog) analog output.

Internal functions and output signal timing can be changed by modifying registers directly via 2-wire serial interface called I2C or by programming the internal/external ROMs which contain device settings.



[Fig. 1] Block Diagram

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