Crystal Image through
Imaging Innovation

PIXELPLUS

Brief Datasheet

1/2.9" HD class Single Chip HD-CVI CMOS Image Sensor with 1280x720 Pixel Array

PV1100K

Rev 0.0

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▶ Features

▷ 1296 x 736 effective pixel array with RGB bayer color filters and micro-lens.
▷ Power supply : HVDD/AVDD=3.3V
▷ Input. Clock Frequency : 27MHz
▷ Output :
◆ Digital Output format :
- max. HD (1280x720) YCbCr422/RGB565/ RGB444. (progressive, 30 fps @ 74.25MHz)
- max. HD (1280x720) Bayer (progressive, 60 fps @ 74.25MHz)
◆ Digital Output interface :
- 16/20 Bits parallel with SMPTE296M
- 8/10 Bits Parallel interface YCbCr422/RGB565/RGB444
◆ Analog Output interface :
- HDCVI (25/50 fps @ 120MHz, 30/60 fps @ 144 MHz)
▷ Image processing on chip : lens shading, gamma / defect / color correction, low pass filter, color interpolation, saturation, edge enhancement, brightness, contrast, special effects, auto black level , auto white balance, auto exposure control and back light compensation.
▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus.
▷ Free scaling(up & down).
▷ Smart contrast, selective color shift
▷ High Image Quality and Ultra low light performance.
▷ I2C,SPI master include.
▷ Motion detection, Privacy mode support
▷ Artificial Intelligence power save mode.
▷ Chip Address Selection PADs
▷ Horizontal / Vertical mirroring.
▷ cropping.
▷ 50Hz, 60Hz flicker automatic cancellation.
▷ Software Reset.
▷ Smart IR-LED control.
▷ Crystal input support.
▷ CLCC/PLCC Package type supports

Pixel Size	4.20 um x 4.20 um
Effective Pixel Array	1296 (H) x 736 (V)
Effective Image Area	5.443 mm x 3.091 mm
Optical Format	1/2.9 inch
Input Clock Freq.	27MHz
Output Format	YCbCr422
Max. Frame rate	74.25MHz @ 60fps SMPTE296M 74.25MHz @ 60fps Bayer 144.0MHz @ 60fps HDCVI
Dark Signal	36.8 [mV/sec] @ 60℃
Sensitivity	5.0 [V/Lux.sec]
Power Supply	Analog & HVDD : 3.3V DVDD : 1.5V
Power Consumption	788.4 mW @ Dynamic (30fps) 763.3 mW @ Dynamic (25fps)
	142.3 uW @ Standby
Operating Temp. (Fully Functional Temp)	-40 ~ 85 [℃]
Dynamic Range	61.2 [dB]
SNR	43.1 [dB]

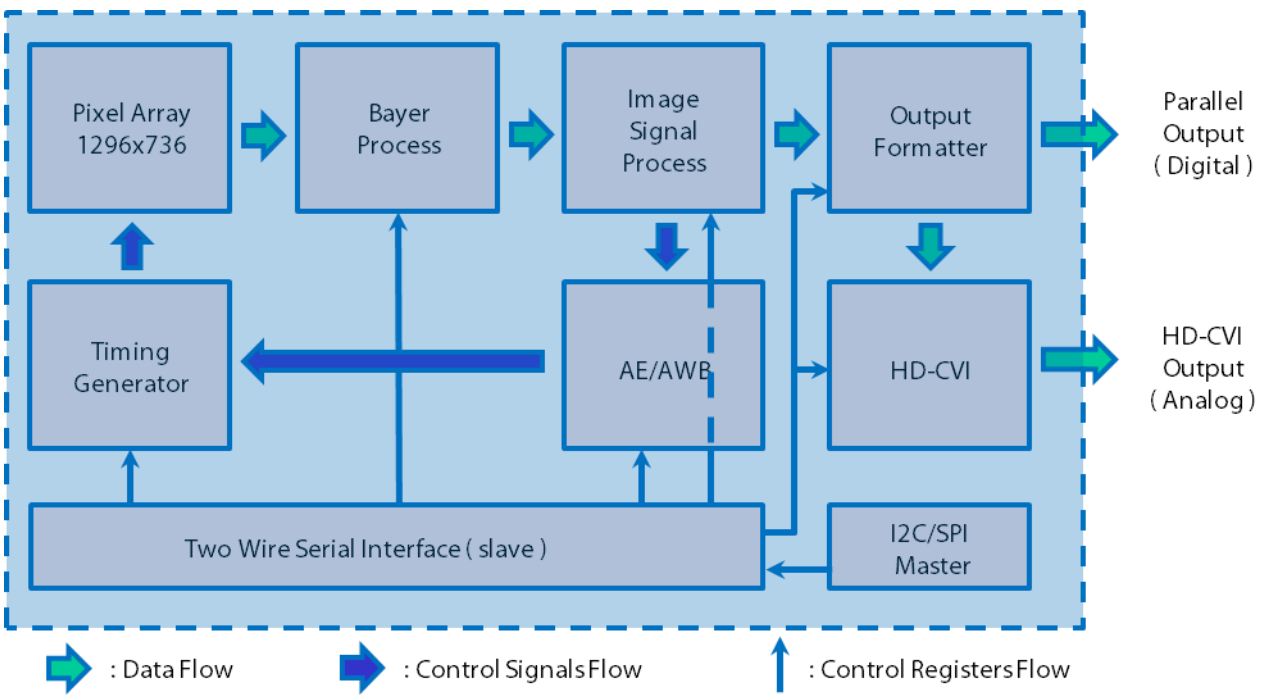
[Table 1] Typical Parameters

▶ Signal Environment

PV1100K doesn't have tolerant Input pads. The input signal must be equal to HVDD for stable operation. If the power of input signal is higher than recommended, it may flow leakage current by shot circuit path in the input PADs.

▶ Chip Architecture

PV1100K has 1296 x 736 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface or SPI interface.



[Fig. 1] Block Diagram

(주)픽셀플러스

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