Crystal Image through
Imaging Innovation

PIXELPLUS

Brief Datasheet

1/2.9" Full HD class Bayer Chip CMOS Image Sensor with 1920x1080 Pixel Array

PS1210K

Rev 0.0

Last Update : 10. June. 2015

6th Floor, 105, Gwanggyo-ro, Yeongtong-gu, Suwon-si, Gyeonggi-do, 443-270, Korea
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▶ Features

▷ 1936 x 1096 Effective pixel array with RGB bayer color filters and micro-lens.

▷ Power supply :
HVDD/AVDD=3.3V

▷ Input. Clock Frequency : 27MHz

▷ Output
◆ Digital Output format
- 10bits RGB Raw Bayer
◆ Digital Output interface
- sub-LVDS
- 10 bits parallel

▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus

▷ High Image Quality
And Ultra low light performance

▷ Chip Address Selection PAD

▷ Horizontal / Vertical mirroring

▷ cropping

▷ Software Reset

▷ External Sync (Gen. Lock) support

▷ Crystal input support

▷ On chip regulator for DVDD

▷ CLCC/PLCC Package type supports

Pixel Size	2.80 um x 2.80 um
Effective Pixel Array	1936 (H) x 1096 (V)
Effective Image Area	5.420 mm x 3.068 mm
Optical Format	1/2.92 inch
Input Clock Freq.	27MHz
Output Clock Freq.	74.25MHz @ 10bit parallel 111.375MHz @ 4ch LVDS
Output Format	10 bits RGB Raw Bayer
Max. Frame rate	30 fps @ sub-LVDS
Dark Signal	12.7 [mV/sec] @ 60℃
Sensitivity	2.0 [V/Lux.sec]
Power Supply	Analog & IO : 3.3V Core : 1.5V (on chip LDO)
Power Consumption	197.0 mW @ Dynamic (Parallel) 244.0 mW @ Dynamic (LVDS)
	330.0 uW @ Standby
Operating Temp. (Fully Functional Temp)	-30 ~ 80 [℃]
Dynamic Range	70.5 [dB]
SNR	43.2 [dB]

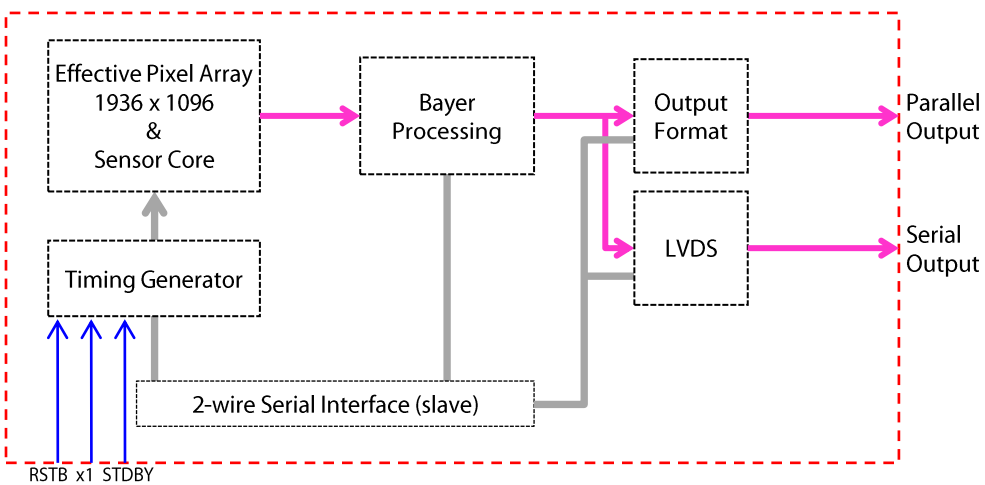
[Table 1] Typical Parameters

▶ Signal Environment

PS1210K don't have tolerant Input pads. The input signal must be equal to HVDD for stable operation. If the power of input signal is higher than recommended, it may flow leakage current by shot circuit path in the input PADs.

▶ Chip Architecture

PS1210K has 1936 x 1096 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.



[Fig. 1] Block Diagram

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