PIXELPLUS CO., LTD.

1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel array

PO8030D

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1/8 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel array

▶ Features

▷ 648 x 488 effective pixel array with RGB Bayer color filters and micro-lens

▷ Power supply
AVDD : 2.8V, DVDD : 1.5V/1.8V
HVDD : 1.5 ~ 3.3V

▷ Output formats
CCIR656, RGB565, 8bits YCbCr422, 8bits RGB Bayer, 8bits Mono

▷ Image processing on chip
Lens shading, Gamma correction, Defect correction, Low pass filter, Color interpolation, Edge enhancement, Color correction, Brightness, Contrast, Saturation, Auto black level compensation, Auto white balance, Auto exposure control and Back light compensation

▷ Max. 30 frame/sec progressive scan @ 24Mhz master clock for VGA

▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus

▷ VGA / QVGA / QQVGA / CIF / QCIF / QQCIF Scaling

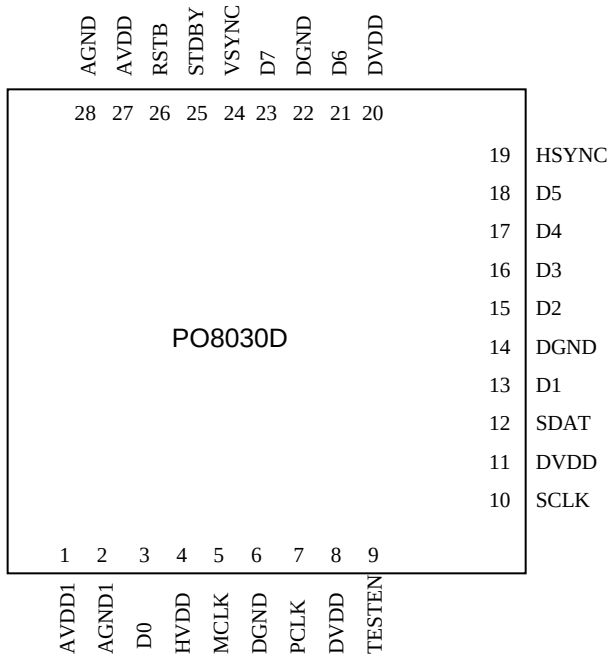
▷ Horizontal / Vertical mirroring

▷ 50Hz, 60Hz flicker automatic cancellation

▷ Software Reset

▷ High Image Quality and High low light performance

▷ Large angle response



[Fig. 1] PIN Description

Effective Pixel Array	648(H) x 488(V)
Pixel Size	2.8 um x 2.8 um
Effective Image Area	1.814 mm x 1.366 mm
Optical Format	1/8 inch
Max. Clock frequency	24 Mhz
Max. Frame Rate	Variable up to 30 fps
Dark Signal	20.5 [mV/sec]
Sensitivity	1.06 [V/Lux.sec]
Power Supply	Analog : 2.8V, Core : 1.5V/1.8V IO : 1.5V ~ 3.3V
Power Consumption	58.7 [mW] @ Dynamic
	4.5 [uW] @ Standby
Operating Temp. (Fully Functional Temp.)	- 40 ~ 105 [°C] @ AT
	- 30 ~ 80 [°C] @ CT
Dynamic Range	60.3 [dB]
SNR	40.8 [dB]

[Table 1] Typical Parameters

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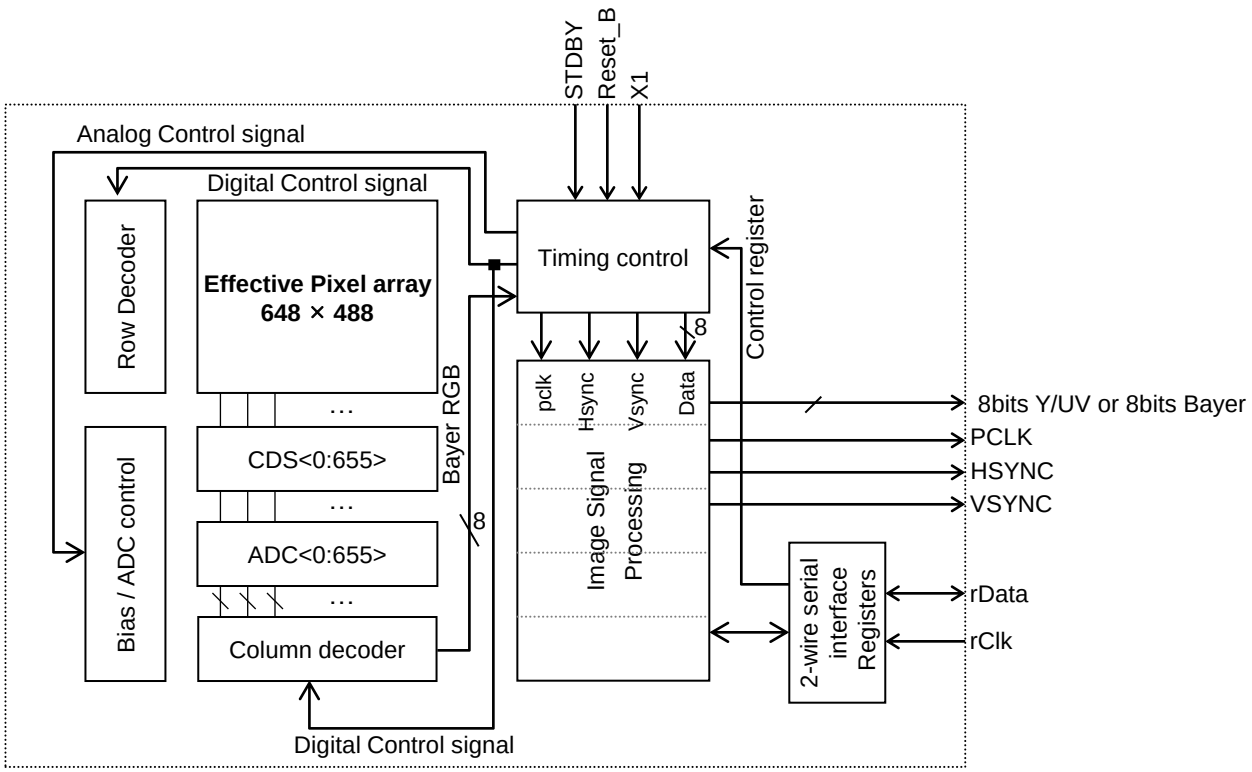
▶ Signal Environment

PO8030D has 3.3V tolerant Input pads. Input signals must be higher than or equal to HVDD but cannot be higher than 3.3V. PO8030D input pad has built in reverse current protection circuit, which makes it possible to apply input voltage even if the HVDD is disconnected or floating. Voltage range for all output signals is 0V ~ HVDD.

▶ Chip Architecture

PO8030D has 648 x 488 total pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.



[Fig. 2] Block Diagram