Crystal Image through
Imaging Innovation

PIXELPLUS

Brief Datasheet

1/2.9" HD Single chip CMOS Image Sensor with 1312x740 Pixel Array

PO3100K

Rev 1.0

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▶ Features

▷ 1312 x 740 effective pixel array with RGB Bayer color filters and micro-lens.
▷ Power supply : 3.3V
▷ Input. Clock Frequency : 27MHz
▷ Output formats
  ◆ Digital Output format
    - max. HD (1280x720) YCbCr422/RGB565/ RGB444 (progressive, 30 fps @ 74.25MHz)
    - max. HD (1280x720) SMPTE296M (progressive, 60 fps @ 74.25MHz)
    - max. HD (1280x720) Bayer (progressive, 60 fps @ 74.25MHz)
  ◆ Digital Output interface
    - 20/16 Bits parallel with SMPTE296M
    - 8/10 Bits Parallel interface YCbCr422/RGB565/RGB444/Bayer
▷ Image processing on chip : lens shading, gamma / defect /color correction, low pass filter, color interpolation, edge enhancement, brightness, contrast, de-color, special effects, auto black level , auto white balance, auto exposure control and back light compensation.
▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus
▷ Free scaling(up & down) / Cropping & Zoom
▷ High Image Quality and High low light performance
▷ I2C / SPI master included
▷ Motion Detection support
▷ On-chip phase locked loop (PLL)
▷ Horizontal / Vertical mirroring
▷ 50Hz, 60Hz flicker automatic cancellation
▷ Software Reset
▷ Smart IR-LED controller
▷ Crystal input support
▷ On Chip regulator for DVDD
▷ CLCC/PLCC Package type supports

Parameter	Typical Value
Effective Pixel Array	1312 (H) x 740 (V)
Pixel Size	4.20 um x 4.20 um
Effective Image Area	5.51 mm x 3.10 mm
Optical Format	1/2.9 inch
Input. Clock Freq.	27 MHz
Output. Clock Freq.	74.25MHz
Output Interface	- 20/16 Bits parallel - 8/10 Bits Parallel interface
Max. Frame Rate	30 fps @ 1280x720, YCbCr 60 fps @ 1280x720, YCbCr 60 fps @ 1280x720, Bayer
Power Supply	AVDD & HVDD : 3.3V
Power Consumption	257.0 mW @Dynamic
	429.0 uW @Standby
Operating Temp. (Fully Functional Temp)	-40 ~ 105 [℃]
Dark Signal	29.2 [mV/sec] @ 60℃
Sensitivity	4.6 [V/Lux.sec]
Dynamic Range	64.8 [dB]
SNR	41.9 [dB]

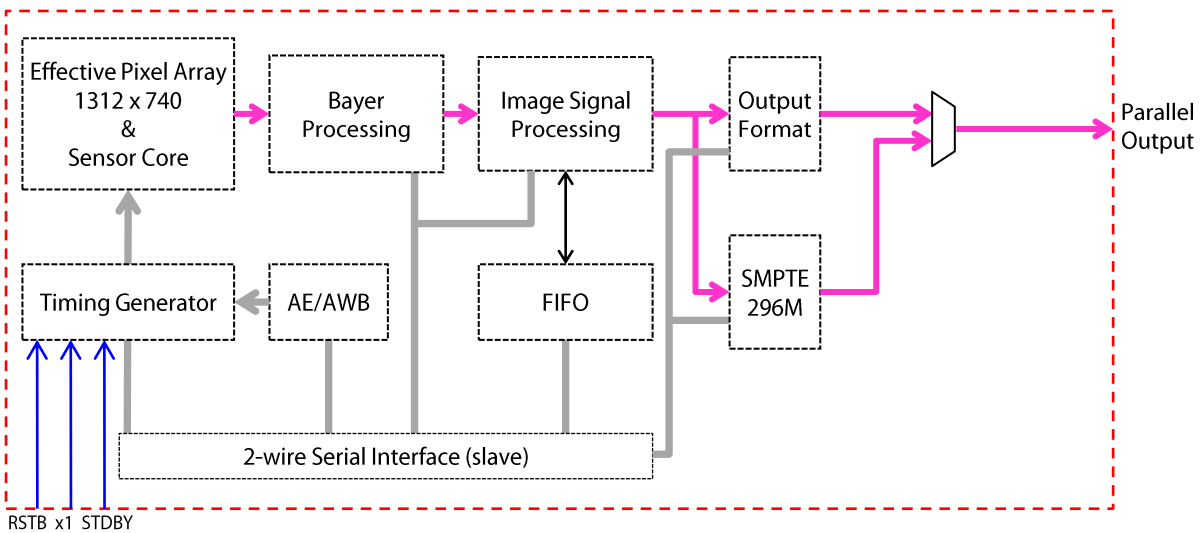
[Table 1] Typical Parameters

▶ Signal Environment

PO3100K don't have tolerant Input pads. The input signal must be equal to HVDD for stable operation. If the power of input signal is higher than recommended, it may flow leakage current by shot circuit path in the input PADs.

▶ Chip Architecture

PO3100K has 1312 x 740 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.



[Fig. 1] Block Diagram

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