PIXELPLUS CO., LTD.

1/3.6 inch 1.5Mega Single Chip CMOS Image Sensor with 1440 X 1024 Pixel array

PO1150K

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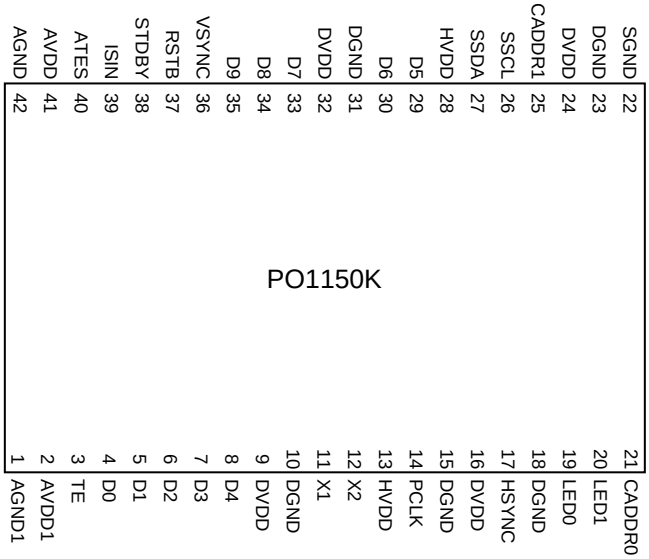
▶ Features

- ▷ 1456 x 1040 effective pixel array with RGB Bayer color filters and micro-lens
- ▷ Power supply
  AVDD : 2.8V, DVDD : 1.8V
  HVDD : 1.8 ~ 3.3V
- ▷ Output formats
  CCIR656, 8bits YCbCr422,
  8bits RGB Bayer, RGB565, RGB444,
  8bits Mono,10bits Raw Bayer
- ▷ Image processing on chip
  Lens shading, Gamma correction, Defect correction, Low pass filter, Color interpolation, Edge enhancement, Color correction, Brightness, Contrast, Saturation, Auto black level compensation, Auto white balance, Auto exposure control and Back light compensation. Special effect (Reverse, Sketch, Sepia, Embossing, Black & White)
- ▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus
- ▷ High Image Quality and High low light performance
- ▷ Shutter type : ERS (Electrical Rolling Shutter)
- ▷ Scan mode : Progressive Scan
- ▷ Variable Image resolution supports
- ▷ Down scaling supports
  x1/8 ~ x1 : 1/32 steps for X, Y respectively
- ▷ Support 1280x720 Bayer image size, for High Definition (HD) 15 fps video systems
- ▷ Support 720x480p YUV 30 fps for D1 systems
- ▷ On-chip phase locked loop (PLL)
- ▷ Horizontal / Vertical mirroring
- ▷ 50Hz, 60Hz flicker automatic cancellation
- ▷ Software Reset
- ▷ Off-chip IR-LED control
- ▷ Motion detection support (64-area)
- ▷ Chip address selection PAD
- ▷ CSP/CLCC/PLCC Package type supports



[Fig. 1] PIN Description

Effective Pixel Array	1456(H) x 1040(V)
Pixel Size	2.8 um x 2.8 um
Effective Image Area	4.0768 mm x 2.912 mm
Optical Format	1/3.6 inch
Max. Clock frequency	48 MHz
Max. Frame Rate	15 fps @ YUV, 1440x1024, 48MHz 15 fps @ Bayer, 1440x1024, 48MHz 30 fps @ YUV, 720x480, 48MHz
Dark Signal	15.5 [mV/sec] @ 60°C
Sensitivity	1.33 [V/Lux.sec]
Power Supply	Analog : 2.8V, Core : 1.8V IO : 1.8V ~ 3.3V
Power Consumption	159.2 [mW] @ Dynamic
	15 [uW] @ Standby
Operating Temp. (Fully Functional Temp.)	- 40 ~ 105 [°C] @ AT
	- 30 ~ 80 [°C] @ CT
Dynamic Range	66.7 [dB] @ 30 fps
SNR	42 [dB]

[Table 1] Typical Parameters

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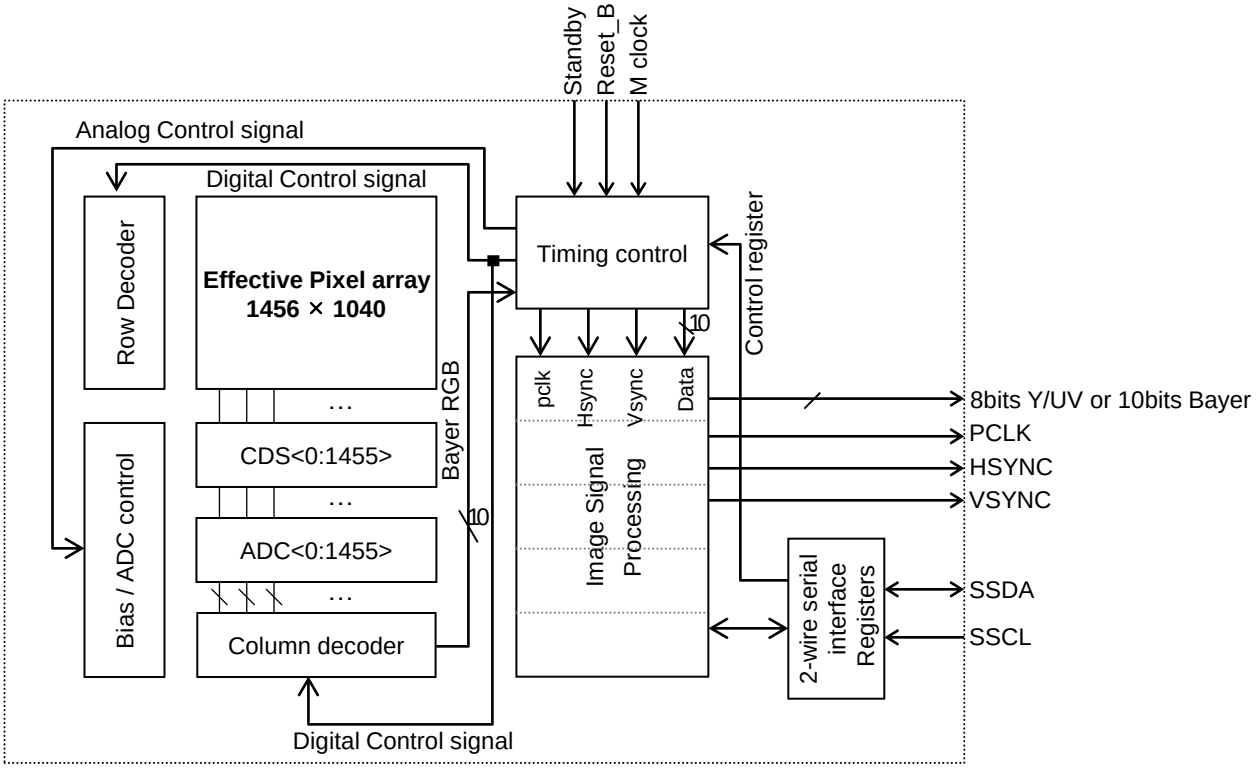
▶ Signal Environment

PO1150K has 3.3V tolerant Input pads. Input signals must be higher than or equal to HVDD but cannot be higher than 3.3V. PO1150K input pad has built in reverse current protection circuit, which makes it possible to apply input voltage even if the HVDD is disconnected or floating. Voltage range for all output signals is 0V ~ HVDD.

▶ Chip Architecture

PO1150K has 1456 x 1040 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.



[Fig. 2] Block Diagram