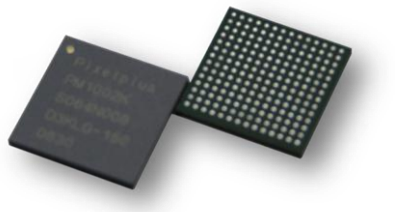
Brief Sheet



Rev 2.0
27. October. 2008

*Image*ARM Processor
(200MHz 32bit RISC Processor)

PM1002K-A196 (Single)
PM1002K-B196 (MCP)
Pin-to-Pin Compatible

6th Floor, Gyeonggi-do R&DB Center, 906-5 Iui-dong, Yeongtong-gu, Suwon-si, Gyeonggi-do 443-766, Korea
Tel: 82-31-888-5300. Fax: 82-31-888-5398. http://www.pixelplus.com

Features

Architecture

- 32-bit RISC 200MHz CPU (FA526 Core/Compatible with ARMv4)
  FA526 is similar to ARM926. FA526 Technology is Micro-Architecture on general ARM Core. Micro-Architecture Technology makes better Mini-Size and Low-Power consumption.
- Instruction-cache (16KB) / Data-cache (16KB)
- Instruction-TCM (4KB) / Data-TCM (4KB)
- Internal-SRAM (64KB)
- AMBA 2.0, AHB/APB
- MMU to support WinCE, Symbian and Linux
- Package
  PM1002K-A196 (Single : 12mm X 12mm, 0.8mm pitch 196 ball pin)
  PM1002K-B196 (MCP: 12mm X 12mm, 0.8mm pitch 196 ball pin, NOR Flash 1MB and Low-Power SDRAM 8MB Included)

System Manager

- Address space : 512 MB SDRAM, 16 MB for 7 banks
- Little/Big Endian support
- Memory banks
  - ✓ 7 banks for SRAM type, SSMC, ROM and others
  - ✓ Two memory banks for SDRAM
  - ✓ Nand Flash BootLoader(16KB)

Operating Conditions

- Internal: 1.8 V
- External I/O: 3.3V (Changeable)
- Speed: 200 MHz @ 1.8V
- Memory: 1.8V/2.5V/3.0V memory

On-chip Peripherals

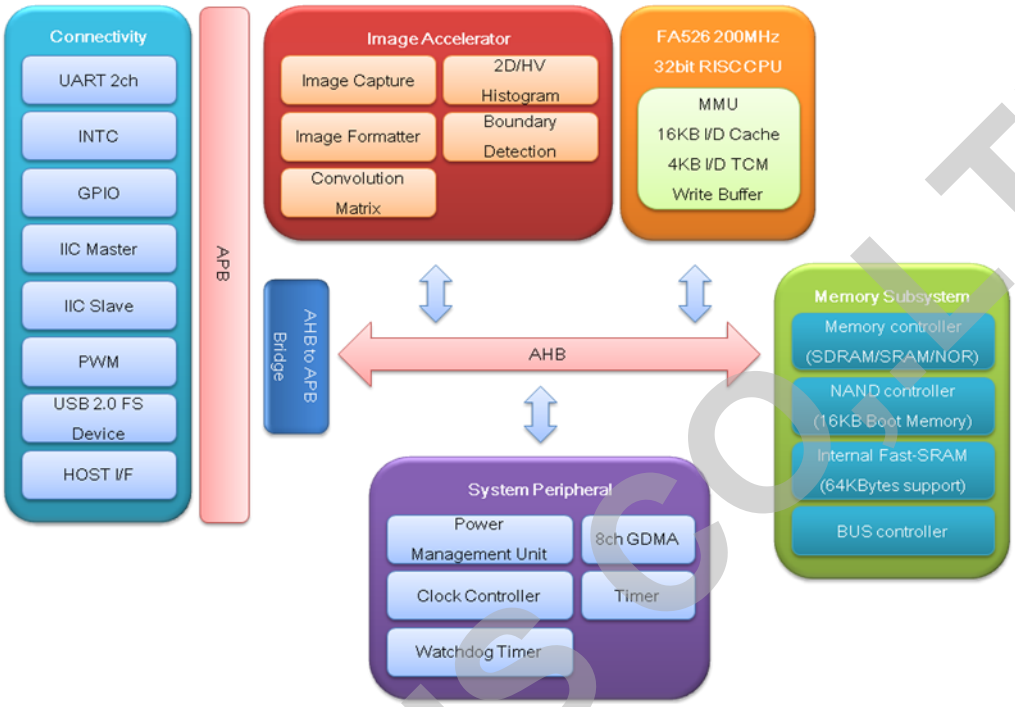
- **Power management : Normal, Idle, Stop, Sleep Mode**
- **Direct Camera Interface**
- **USB 2.0 FS Device**
- **1-ch IIC Master, 1-ch IIC Slave**
- **On-chip Clock Generator with PLL**
- **2-ch UART**
- **32bit Watch-Dog Timer**
- **84 General Purpose I/O Ports**
- **4-ch Timers, 2-ch PWM Timers**
- **Host Interface (if connected to baseband)**
- **64 KBytes Internal Fast SRAM**
- **NAND Controller (16 KBytes Nand-Boot Memory)**
- **8-ch Scatter-Gathered DMA : memory↔memory, peripheral↔memory**
- **Hardware Image Accelerator :**
  Image Capture, Matrix Convolution, 2D/HV Histogram, Boundary Detection, Image Formatter
- **Boot Modes : NOR Flash, NAND Flash, IIC Slave, 8-bit ROM Modes Supported**
- **Power : Low-Power Architecture Adopted**
  Normal (100 mW), Idle (1 mW), Idle current (0.4 mA)

Key Application

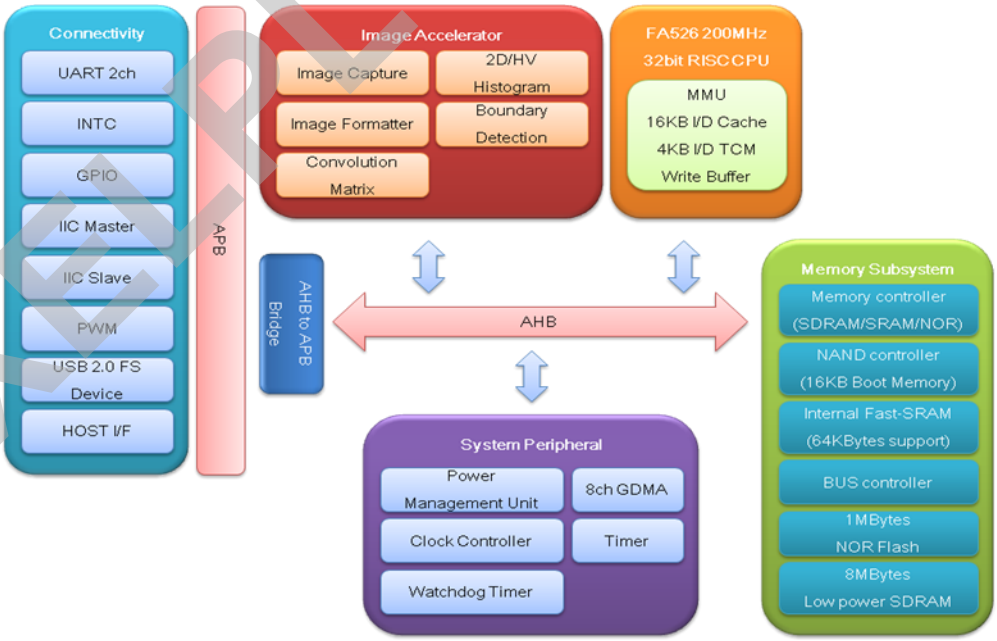
- **CMOS Image Sensor + MCU Application**
- **PDA/Smart Phone (Image Recognition)**
- **Intelligent Video Analytics System (CCTV, IP Camera)**
- **Biometrics (Face, Iris, Fingerprint)**
- **Vehicles Number Recognition**
- **DVR**
- **Security Application**

Block Diagram

PM1002K-A196



PM1002K-B196



Block Descriptions

32-BIT RISC PROCESSOR FA526

This core is an ultra-high speed general-purpose 32-bit embedded RISC processor.
It can operate at a speed up to 200 MHz in the low power consumption. It includes separated 32 KB instruction/32 KB data caches, separated instruction/data scratch pads (=TCM), a write buffer, a memory management unit and a JTAG ICE interface.
The CPU core is a Harvard architecture design with 8 pipeline stages consisting of Fetch, Instruction, Decode, Register Access, Shift, Execution, Memory and Write stages. To reduce the branch penalties, it contains a Branch Target Buffer (BTB) and a Return Stack (RS) to improve the overall performance. MMU provides the address translation and permission check mechanisms for the memory access.

MEMORY CONTROLLER

The Memory Controller supports the flash memory, SDRAM, SRAM or ROM.
Memory Controller features include:

- External Memory Address space
  - ✓ ROM/SRAM/IO Area : Max 16M bytes for each bank (total 128M bytes)
  - ✓ SDRAM/SRAM Area : Max 256M bytes for each bank (total 512M bytes)
  - ✓ Embedded SRAM Address space : 64K bytes
  - ✓ NOR Flash Memory Address space : Up to 16M bytes
  - ✓ Pseudo SRAM Memory Address space : Up to 16M bytes
  - ✓ Supports programmable 8/16/32 bit data bus width for each bank (Embedded SRAM = 32 bit data bus width)
- Fully Programmable access cycles for all memory banks
- Supports external wait signals to expend the bus cycle
- Supports self-refresh mode in SDRAM for power Down
- Frame Memory Access : Single and Burst Read/Write (Burst Size = 16)

Direct Memory Access Controller (DMAC)

The DMAC provides enhanced system performance. The system efficiency is improved by the high-speed data transfers among the system and devices and by reducing the processor-interrupt generation. The DMAC provides up to 8 channels for the memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers with the shared buffers.
The DMAC features include:

- Provides the memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers
- Group round-robin arbitration scheme with 4 priority levels
- Supports chain transfer
- Supports transfer with 8-/16-/32-bit data width

Enhanced NAND Flash Memory Controller (NANDC)

The NAND Flash host controller provides an interface to access the NAND type flash.
The NAND type of flash is the most cost-effective solution for large nonvolatile storage applications including the digital voice recorders, digital still cameras, and other portable applications requiring non-volatility.

- Supports booting from NAND flash memory.
- 64KB internal buffer for booting.
- Supports storage memory for NAND flash memory after booting.
- Supports Advanced NAND flash

Power Management Unit (PMU)

The clock & power management block consists of two parts: clock control and power control.
The Clock control logic in PM1002K can generate the required clock signals including FCLK for CPU, HCLK for the AHB bus peripherals, and PCLK for the APB bus peripherals. The PM1002K has one Phase Locked Loops (PLLs) for FCLK, HCLK, and PCLK. The clock control logic can make slow clocks without PLL and connect/disconnect the clock to each peripheral block by software, which will reduce the power consumption.

- Power Control Logic is divided the Normal Mode, Slow Mode, Power Down Mode and Sleep Mode.
  - ✓ Normal Mode :
    the block supplies clocks to CPU as well as all peripherals in the PM1002K. In this mode, the power consumption will be maximized when all peripherals are turned on. It allows the user to control the operation of peripherals by software. For example, if a timer is not needed, the user can disconnect the clock to the timer to reduce power consumption.
  - ✓ Slow Mode :
    FCLK for CPU is generated by SLOWCON (Slow Clock Generation Register) and it does not use PLL Block.
  - ✓ IDLE Mode :
    The block disconnects clocks (FCLK) only to the CPU core while it supplies clocks to all other peripherals. The IDLE mode results in reduced power consumption due to CPU core. Any interrupt request to CPU can be woken up from the Idle mode.
  - ✓ Sleep Down Mode :
    All internal blocks are disconnected from clock source with the exception of wake-up logic block.
- On-chip clock generator with PLL
- Clock sources from the AHB or APB Block can be masked, that is, it is designed to reduce the power consumption by masking all unused clocks.

Image Capture Unit

The Image Capture Unit saved Image data from Image Sensor to Frame Memory.
This block is able to program image size and position to save.
Also supports to input of Bayer image format and performs Color interpolation.
The Image Capture Unit features include:

- CIS Gray or Bayer Image Image-Capture.
- Programmable Sample size.
- Sub sample mode with Gray or Bayer.
- Inter-polation function.
- Programmable Read/Write Memory address for image data.
- input source select
- Output select from interpolation, Frame Memory data, CIS Sub-sample
- Memory write select from interpolation, CIS Sub-sample.
- (Max frame rate depends by bus or memory)
- Interpolation select from CIS Sub-sample, memory read
- Programmable active size for read of image data in memory.
- two operation mode with CIS input
- Single frame mode, repeat mode.
- Max operation 100Mhz.
- AMBA Master Interface.

General Histogram (2D histogram)

The 2D histogram is an unit to computes a number of pixels for each grey level within an image from the image sensor in real time. Images saved in the frame memory can be computed in the same manner. When the process is completed, an interrupt can be trigged. The Histogram can be given if frame memory is assigned. If related registers are set with appropriate values in order to clear the assigned memory areas, it is done by HW within 256 Cycle

Conditional Histogram (HV histogram)

The Conditional histogram counts a number of pixels that contains vertically and horizontally designated gray values in an image from the image sensor. The size of horizontal and vertical areas is programmable. The Conditional histogram can be used to find a location of a specific image feature.

- Supports real time histogram from image capture engine (Max data rate :50Mbyte/sec)
- Programmable active size.
- Supports two histogram by threshold range:
- Binary horizontal histogram, Binary vertical histogram
- Supports Run with initial memory function
- Max operation 100Mhz

Boundary Detect Unit

The Boundary Detector Unit has a function of obtaining pixels' information at the point of sharp change in the 640x480 size gray image from the image capture unit and save its result in the memory. The sharp change is detected by appropriate values assigned to their respective registers but the values can be changed as circumstances are changed.

- Independent 2ch function
- Gray Image Boundary detection.
  - ✓ one operand simple, two operand combinational condition mode
  - ✓ and, or, xor, nand, nor, xnor operation mode by two operand
- Programmable Memory address.
- Programmable active size.
- Programmable filter fifo size.
- Max operation 100Mhz

Matrix Convolution

The trick of image filtering is that you have a 2D filter matrix, and the 2D image. Then, for every pixel of the image, take the sum of products. Each product is the color value of the current pixel or a neighbor of it, with the corresponding value of the filter matrix. The center of the filter matrix has to be multiplied with the current pixel, the other elements of the filter matrix with corresponding neighbor pixels.

- Supports the image size up to 3×3, 5×5

Image Formatter

Image formatter has a role to bridge instruction and data of an external host via host bus to an internal block. It could directly reach all areas since the Host interface is compliant with AMBA.

- Pullout Memory data.
- Pullout Output after adjusting
- Dedicated input DMA & Video Buffer
- Pullout synchronized Xin_clk or Hclk

I2C

The I2C is a two-wire bidirectional serial bus that provides a simple and efficient method of the data exchange while minimizing the interconnection between the devices. The I2C bus interface controller allows the host processor to serve as a master or slave residing on the I2C bus. The data are transmitted to and received from the I2C bus via a buffered interface.

- I2C master controller
  - ✓ Supports i2c slave function
  - ✓ Supports System Area access and ready flag
  - ✓ Supports slave SCL wait function
  - ✓ Supports SCL, SDA, sample sync function
  - ✓ Supports boot ram access for I2C boot
  - ✓ Supports 8FIFO Rx/Tx
  - ✓ Supports Rx Time out
  - ✓ AMBA APB salved interface

- I2C Slave controller
  - ✓ Supports i2c master function
  - ✓ Supports programmable pulse width
  - ✓ Supports Bus Lose detect function
  - ✓ Programmable acknowledge bit

Host interface

Host interface has a role to bridge instruction and data of an external host via host bus to an internal block. It could directly reach all areas since the Host interface is compliant with AMBA.

- Supporting an access by AMBA AHB master
- Supporting an access by AMBA AHB Slave
- Configuring signals by memory timing.
- Communicating through Interrupt signals.

USB FS Device Controller

Universal serial bus controller supports the USB Full speed (12Mbps).

UART

An UART controller supports serial communication and standard asynchronous communication bits (start, stop, and parity). Baud rates are programmable up to 1152kbps. The characteristics of the UART are listed as below.

- 2-ch UART :
  - ✓ Ch 0 uart 64 bytes FIFO (each RX, TX)
  - ✓ Ch 1 uart nonfifo
- Fully programmable serial interface :
  - ✓ 5-, 6-, 7-, or 8-bit characters
  - ✓ Even, odd, and no parity detections
  - ✓ 1, 1.5 or 2 stop-bit generations

GPIO

GPIO is used for input/output of external data. Each GPIO is programmable to input or output.

- 84 General Purpose I/Os
- Multiplex with Normal Signals
- Useable after Pin Mux Register is set.

Timer

The Timer consists of 6 sub-timers and 2 of them can be assigned for PWM. Each sub-timer does increment counting based on the pclk or xin_clk. It can operate as single or period mode and when the count reaches to appointed value, interrupts can be triggered
The characteristics of the Timer are listed as below.

- 6 independent 32-bit timer programming models
- Interrupts can be issued upon the overflow and time-up
- Each sub-timer has 2 match registers
- Programmable incrementing modes on the counter
- Support single/period mode
- Pclk or xin_clk

PWM

There are 6 sub-timers and 5th and 6th sub-timers are assigned to be used for PWM. The PWM operates based on the setting of Period, Duty, Pulse number and Negative/Positive polarity and it supports auto reload.
The characteristics of the PWM are listed as below.

- 2 independent 32-bit timer programming models
- Trigger interrupts after receiving the appointed pulse numbers of PWM signals
- Each sub-timer has 2 match registers
- Programmable incrementing modes on the counter
- Support single/period mode
- Auto Reload
- Apb_clk or xin_clk

OSCR(Operation System Counting Register)

The OSCR is designed to up count until it reaches appointed time and when 32bit is full of data, it restarts the counting from '0'. The interval is computed by pre-scaling the Xin_clk.
The OSCR features include:

- 32-bit counter
- Each sub-timer has 1 match registers

Watch Dog Timer (WDT)

The WDT is used to prevent the system from infinite looping if the software becomes trapped in a deadlock. In the normal operation, the user restarts the WDT at the regular intervals before the counter counts down to zero. The WDT generates one or a combination of the following signals: reset or interrupt. The WDT selects operation clock either apb_clk or xin_clk.
The WDT features include:

- 32-bit down counter
- Upon timeout, WDT outputs one or a combination of the System reset/system interrupt

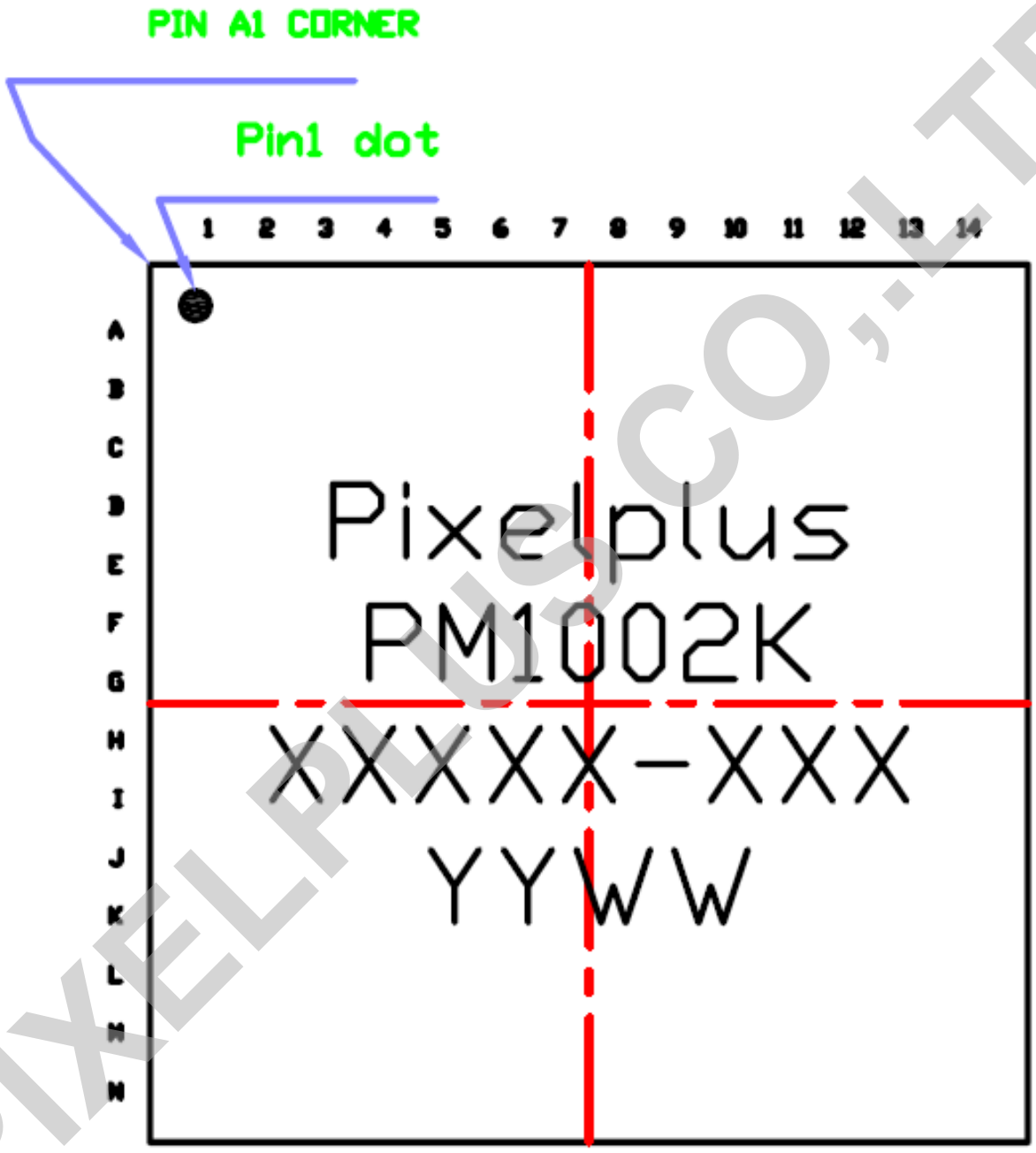
Interrupt Controller (INTC)

The interrupt controller provides both the FIQ and IRQ modes to the microprocessor. It also determines the causes of the interrupts as an IRQ or an FIQ and masks the interrupts.
The INTC features include:

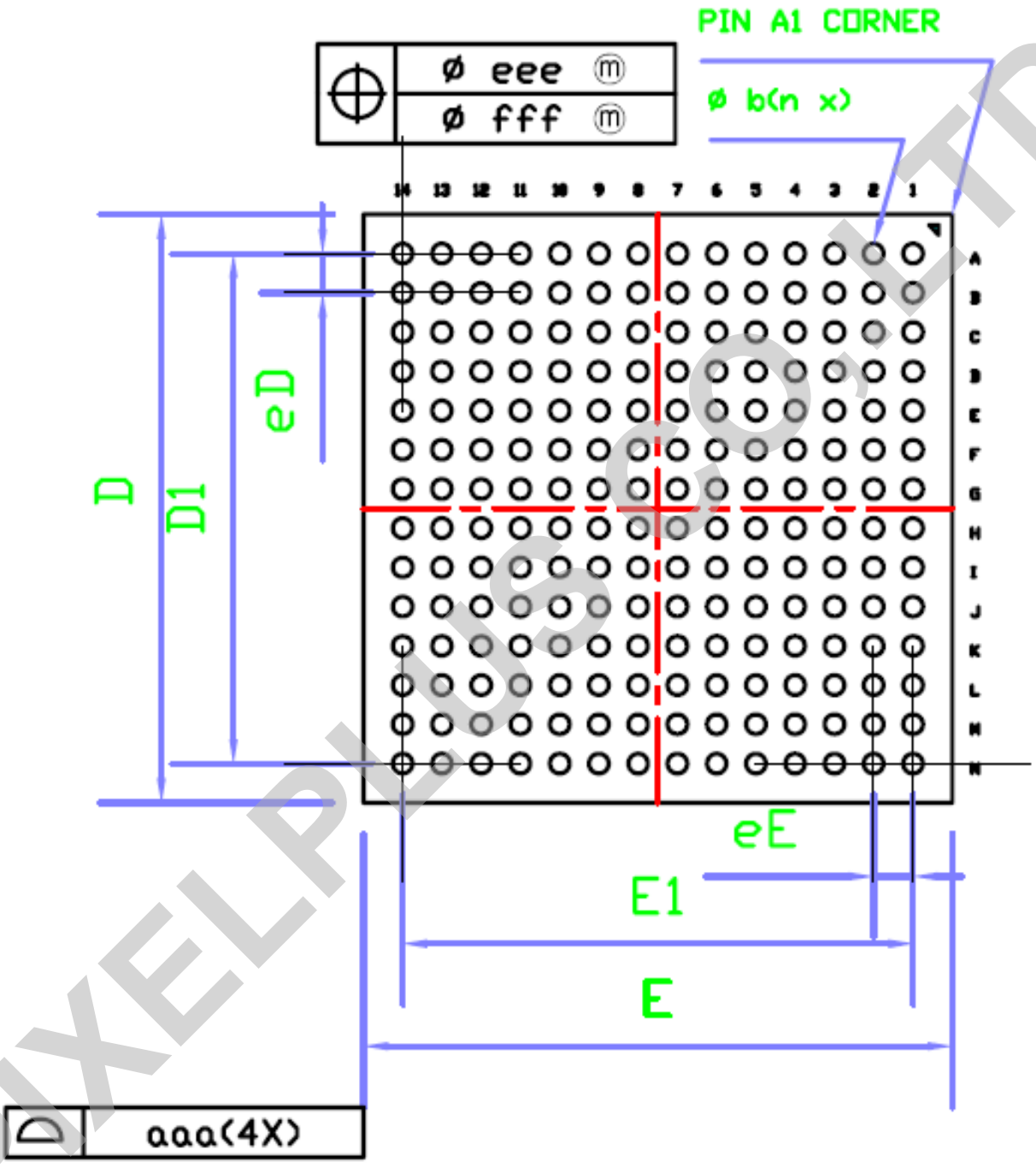
- Supports up to 27 fast interrupt (FIQ) inputs
- Supports up to 27 standard interrupt (IRQ) inputs
- Interrupts can be routed to either the IRQ or FIQ
- Provides both the edge-/level-triggered interrupt sources with the positive and negative directions
- Supports the de-bounce circuits for the interrupt input sources
- Independently enable or disable any interrupt sources
- Provide Global Mask both FIQ and IRQ

Package Information

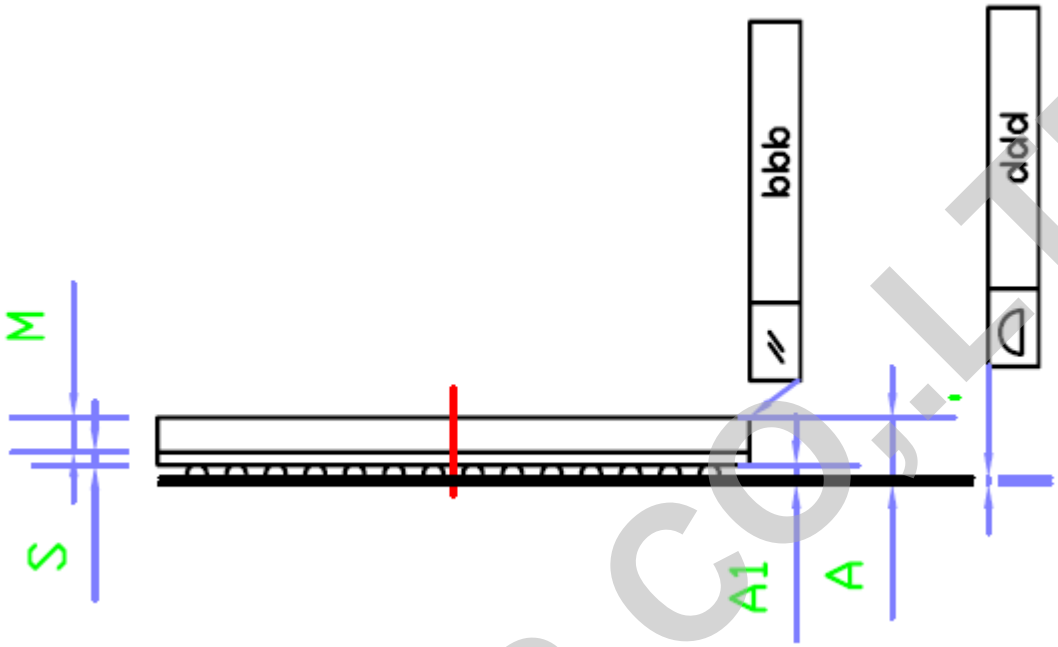
Top View



Bottom View



Side View



		Symbol	Common Dimension
Package			LFBGA
Body Size	X	E	12.000
	Y	D	12.000
Ball Pitch	X	eE	0.800
	Y	eD	0.800
Total Thickness		A	1.40 Max
Mold Thickness		M	0.70 Ref
Substrate Thickness		S	0.26 Ref
Ball Diameter			0.40
Stand Off		A1	0.27 ~ 0.37
Ball Width		b	0.38 ~ 0.48
Ball Count		n	196
Edge Ball Center to Center	X	E1	10.40
	Y	D1	10.40
Package Edge Tolerance		aaa	0.150
Mold Flatness		bbb	0.200
Coplanarity		ddd	0.120
Ball Offset (Package)		fff	0.150
Ball Offset (Ball)		eee	0.080

ARM Tools

Recommended:

- **ARM ADS 1.2 (Current Used)**
- **ARM RVDS 3.0**

Possible:

- **ARM SDT 2.51**
- **IAR**
- **GCC**

※ **Basically, you can use any arm compilers**

JTAG DEBUGGERS

Recommended:

- **OPENice-A1000 (AIJI SYSTEM, Korea)**
- **Trace-32 (Laterbach, Germany)**

Possible:

- **Multi-Ice (ARM)**
- **Etc: Dragon-Ice(China), Faraday-Ice(Taiwan)**

Companies Web Sites

- **ARM :** http://www.arm.com.com
- **AIJI SYSTEM :** http://www.aijisystem.com
- **MDS technology (Trace32 Korean Representative)**
  : http://www.mdstec.com/main/index.asp**,** http://www.trace32.com
- **Faraday :** http://www.faraday-tech.com
- **IAR :** http://www.iar.com