Crystal Image through
Imaging Innovation

PIXELPLUS

Brief Datasheet

FHD Image Signal Processor with On-Chip NTSC/PAL TV Encoder

PI2008K

Rev 0.0

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▶ Features

▷ Power Supply
HVDD/CVDD/AVDD : 3.3V
DVDD = 1.7V

▷ Input. Clock Frequency : 27MHz

▷ Input Interfaces : 10bit parallel/4 channel LVDS

▷ Input Formats : Bayer/YCbCr422

▷ Output Interfaces
- 8/16bit parallel
- CVBS

▷ Output Formats
◆ Composite Output Mode
- NTSC/PAL
◆ Digital Output Mode
- Max. FHD (1920x1080)
YCbCr422/RGB565/RGB444
(progressive, 30fps @ 74.25Mhz)
- ITU-R. BT1302 (960x240/288)
- SMPTE296M
- BT1120

▷ Video frame rate control by Built-in 8MB SDRAM

▷ Image Processing on chip
lens shading, gamma/defect/color correction
low pass filter, color interpolation
Saturation, Edge enhancement
brightness, contrast, special effects
auto black level, auto white balance
auto exposure control and back light compensation

▷ Frame size, Window size and position
Can be programmed through a I2C interface bus
▷ Free scaling (Up&Down)
▷ High Image Quality and
Ultra low light performance

▷ I2C, SPI master include
▷ Motion Detection Support
▷ Alarm mode, Privacy mode support
▷ Artificial Intelligence power save mode
▷ Horizontal/Vertical mirroring
▷ Cropping
▷ 50/60Hz flicker automatic cancellation
▷ Software Reset
▷ Smart IR-LED control
▷ Crystal input support
▷ QFN Package type supports

Frame Rate	**Analog Output** - 60 fields/sec @ NTSC - 50 fields/sec @ PAL **HD** - 30 fps @ YCbCr, 74.25Mhz - 60 fps @ SMPTE296M, 74.25Mhz **FHD** - 30 fps @ YCbCr, 148.5Mhz - 60 fps @ BT1120, 74.25Mhz
Power Supply	Analog : 3.3V HVDD : 3.3V CVDD : 3.3V DVDD : 1.7V
Power Consumption	375.9 mW @ Dynamic (Parallel) 407.1 mW @ Dynamic (LVDS)
	TBD uW @ Standby
Operating Temp. (Fully Functional Temp.)	-40˚C ~ +85˚C

[Table 1] Typical Parameters

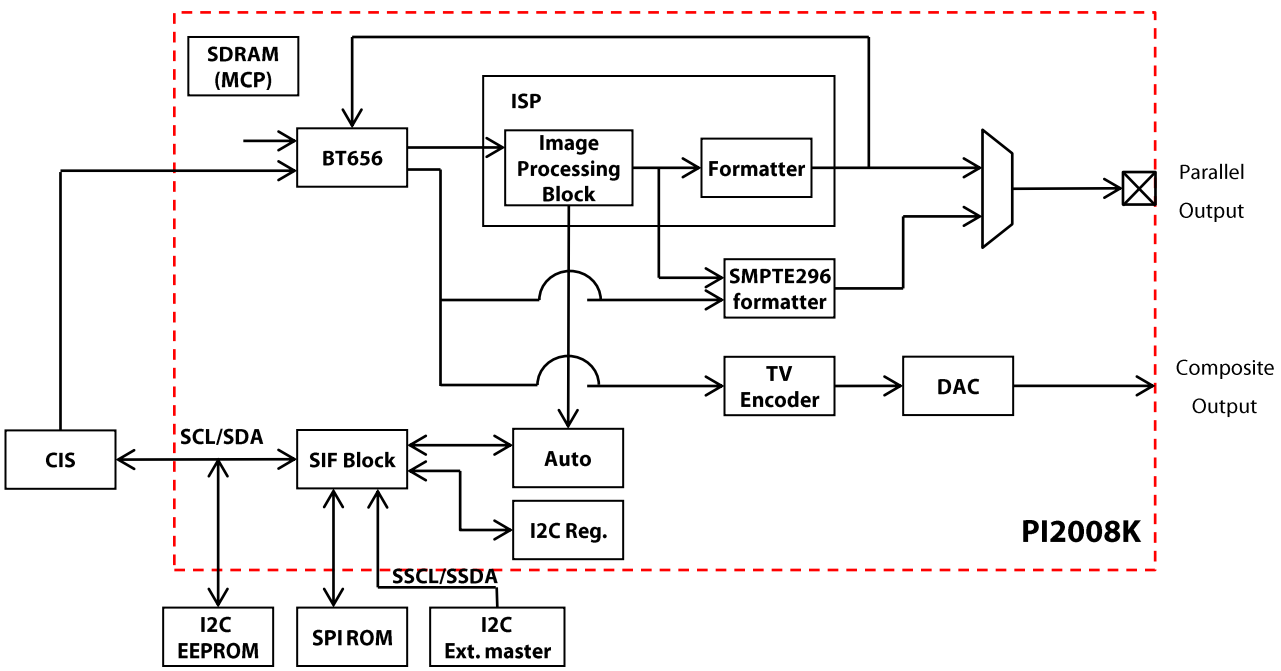
▶ Signal Environment

PI2008K don't have tolerant Input pads. The input signal must be equal to HVDD for stable operation. If the power of input signal is higher than recommended, it may flow leakage current by shot circuit path in the input PADs.

▶ Chip Architecture

PI2008K is a full-HD image signal processor with on-chip NTSC/PAL TV encoder that receives bayer or YCbCr input from an external CIS and transforms it into an digital or NTSC/PAL analog output. A frame buffer stores whole frames of image input to facilitate frame rate conversion from input images of frame-rate less than 30 to TV output of 60 fields per second. PI2008K has a SIF(Serial Interface Controller) block that take care of the system initialization. After reset, SIF reads initialization table stored in a ROM outside and programs control registers in and out.

The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.



[Fig. 1] Block Diagram

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