PIXELPLUS CO., LTD.

# *1/2.9 inch HD class Single Chip CMOS Image Sensor with 1312 X 816 Pixel array*

# PH1100K

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# 1/2.9 inch HD class Single Chip CMOS Image Sensor With 1312 X 816 Pixel array

## ▶ Features

- ▷ 1312 x 816 effective pixel array with RGB Bayer color filters and micro-lens
- ▷ Power supply
  AVDD : 2.8V
  HVDD : 2.8V or 3.3V
- ▷ Output formats
  CCIR656, YCbCr422, RGB565, RGB444
  Raw Bayer, ISP Bayer
- ▷ Image processing on chip
  Lens shading, Gamma correction, Defect correction, Low pass filter, Color interpolation, Edge enhancement, Color correction, Brightness, Contrast, De-color, Auto black level compensation, Auto white balance, Auto exposure control and Back light compensation. Special effects (Reverse, Sketch, Sepia, Embossing, Black & White)
- ▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus
- ▷ High Image Quality and High low light performance
- ▷ I2C / SPI master included
- ▷ 4 layer overlay function by using SPI ROM
- ▷ Scan mode : Progressive Scan
- ▷ On-chip phase locked loop (PLL)
- ▷ Horizontal / Vertical mirroring
- ▷ Cropping & max 4x Digital Zoom support
- ▷ 50Hz, 60Hz flicker automatic cancellation
- ▷ Software Reset
- ▷ Off-chip IR-LED control
- ▷ Motion detection support (64-area)
- ▷ Chip address selection PAD
- ▷ Crystal input support
- ▷ On chip regulator for core
- ▷ CSP/52CLCC/PLCC Package type supports

| | |
|---|---|
| **Effective Pixel Array** | 1312(H) x 816(V) [WXGA] |
| **Pixel Size** | 4.2 um x 4.2 um |
| **Effective Image Area** | 5.51 mm x 3.42 mm<br>(Diagonal 6.48 mm) |
| **Optical Format** | 1/2.9 inch |
| **Input Clock Frequency** | 27 MHz |
| **Output Clock Frequency** | 74.25 MHz (parallel)<br>148.5MB/s (serial) |
| **Output Interface** | • 20/16 bits Parallel with SMPTE296M<br>• 8/10 bits Parallel interface<br>• MIPI Serial interface with 2 lanes (148.5MB/s) |
| **Max. Frame Rate** | 60 fps @ YUV<br>60 fps @ Bayer |
| **Power Supply** | Analog : 2.8V<br>IO : 2.8V or 3.3V<br>Core : 1.5V (On chip LDO) |
| **MAX CRA** | 10 Degree |
| **Applications** | Car Blackbox, HD-CCTV<br>IP CAM, Rear View, Smart TV<br>Door Phone, etc. |
| **Sensitivity** | 6.8 [V/Lux.sec] |
| **Power Consumption** | 595.0 [mW] @ Dynamic |
| | 517.1 [uW] @ Standby |
| **Dynamic Range** | 57.2 [dB] |
| **SNR** | 41.1 [dB] |

[Table 1] Typical Parameters

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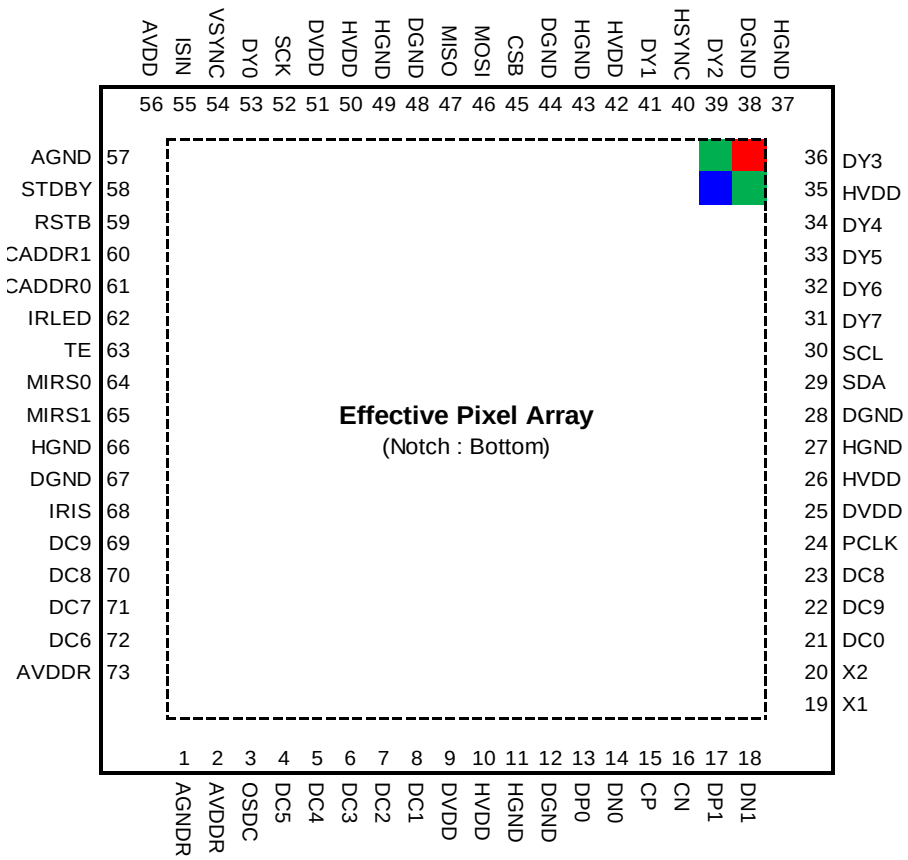
## ▶ PIN Descriptions




[Fig. 1] PIN Description

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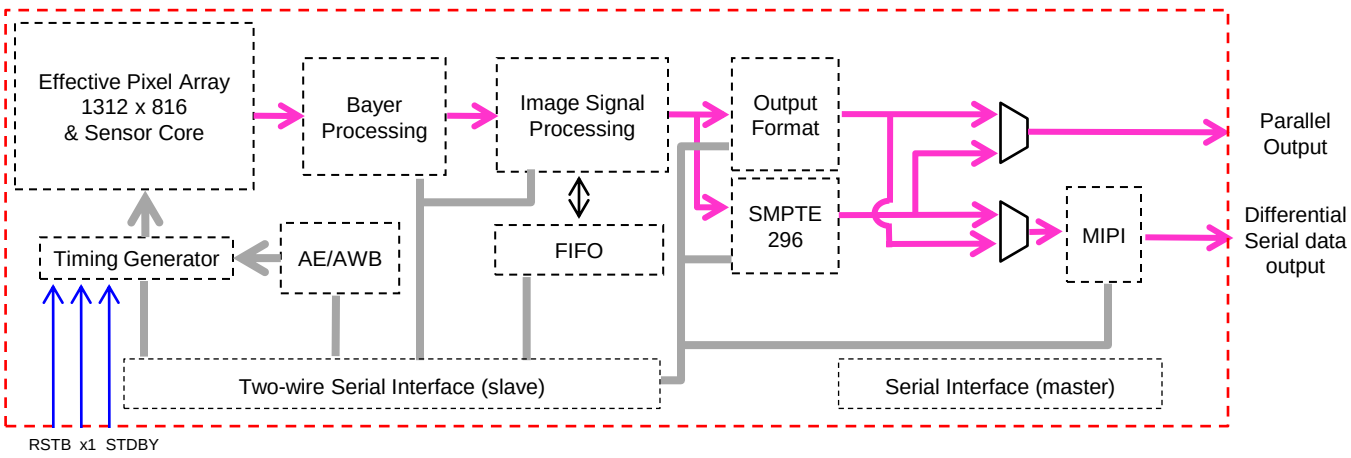
## ▶ Signal Environment

PH1100K don't have tolerant Input pads. The input signal must be equal to HVDD for stable operation. If the power of input signal is higher than recommended, it may flow leakage current by shot circuit path in the input PADs.

## ▶ Chip Architecture

PH1100K has 1312 x 816 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.




[Fig. 2] Block Diagram