Crystal Image through
Imaging Innovation

PIXELPLUS

Brief Datasheet

1/4" NTSC/PAL CMOS Image Sensor with 640x480 Pixel Array

PC7030K

Rev 0.0

Last Update : 10. June. 2015

6th Floor, 105, Gwanggyo-ro, Yeongtong-gu, Suwon-si, Gyeonggi-do, 443-270, Korea
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▶ Features

▷ 648 x 488 Effective pixel array with
RGB bayer color filters and micro-lens.

▷ Power supply :
HVDD/CVDD/AVDD=3.3V

▷ Input. Clock Frequency : 27MHz

▷ Output formats
◆ Composite Output mode :
- CVBS (NTSC/PAL)
◆ Analog/Digital Concurrent Output mode
- ITU-R. BT656 (720x240/288)
(interlaced, 60 fields/50fields @ 27MHz)
- CVBS (30 fps / 25 fps @ 27MHz)

▷ Image processing on chip
lens shading, gamma/defect/color correction
low pass filter, color interpolation, saturation
edge enhancement, brightness, contrast
auto black level, auto white balance
auto exposure control
and back light compensation

▷ High Image Quality
And Ultra low light performance

▷ I2C master include

▷ Chip Address Selection PAD

▷ Horizontal / Vertical mirroring

▷ 50Hz, 60Hz flicker automatic cancellation

▷ Software Reset

▷ IR-LED control with CdS

▷ Crystal input support

▷ On chip regulator for DVDD

▷ CLCC/PLCC Package type supports

Pixel Size	5.60 um x 5.60 um
Effective Pixel Array	648 (H) x 488 (V)
Effective Image Area	3.63 mm x 2.73 mm
Optical Format	1/4 inch
Input Clock frequency	27MHz
Frame Rate	60 field / sec @ NTSC 50 field / sec @ PAL
Dark Signal	38 [mV/sec] @ 60℃
Sensitivity	10.5 [V/Lux.sec]
Power Supply	Analog : 3.3V HVDD : 3.3V CVDD : 3.3V
Power Consumption	312.8 mW @ Dynamic
	391.6 uW @ Standby
Operating Temp. (Fully Functional Temp)	-40 ~ 105 [℃]
Dynamic Range	65.3 [dB]
SNR	46.2 [dB]

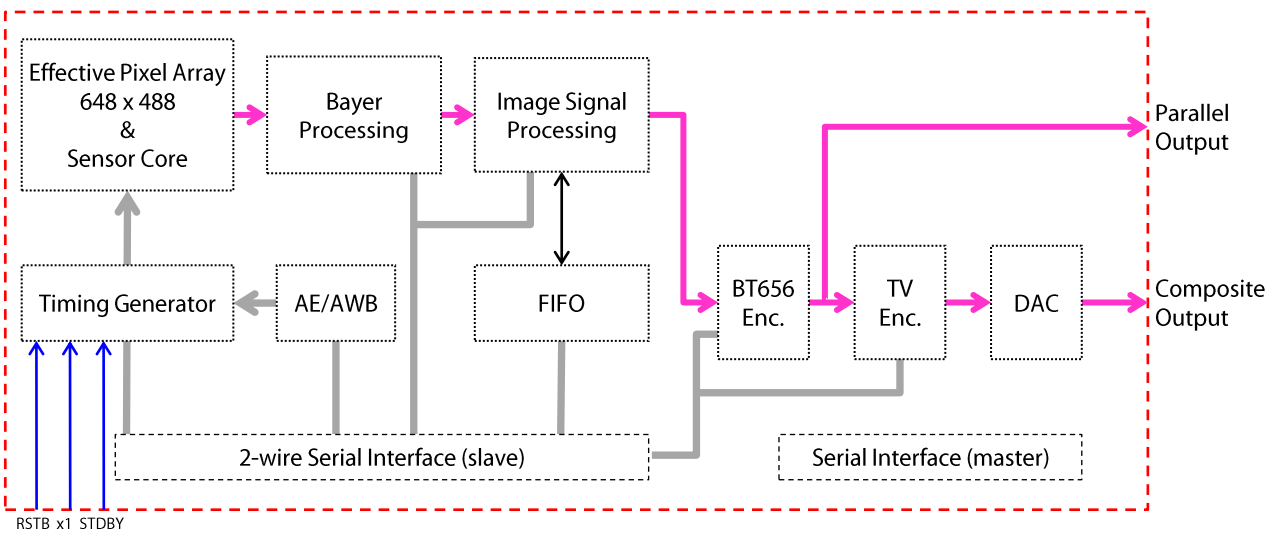
[Table 1] Typical Parameters

▶ Signal Environment

PC7030K don't have tolerant Input pads. The input signal must be equal to HVDD for stable operation. If the power of input signal is higher than recommended, it may flow leakage current by shot circuit path in the input PADs.

▶ Chip Architecture

PC7030K has 648 x 488 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.



[Fig. 1] Block Diagram

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