PIXELPLUS CO., LTD.

# *1/4 inch VGA class Analog/Digital Output NTSC/PAL CMOS Image Sensor*

# PC1030N

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# 1/4 inch VGA class Analog/Digital Output NTSC/PAL CMOS Image Sensor

## ▶ Features

▷ 648 x 488 Effective pixel array with RGB bayer color filters and micro-lens and optical black pixel.

▷ Power supply :
AVDD : 2.8V, CVDD : 2.8V, DVDD : 1.8V,
HVDD : 2.8 ~ 3.3V

▷ Output formats :
CVBS ( NTSC/PAL),
ITU-R. BT601/656
YCbCr422

▷ Image processing on chip :
lens shading, gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, brightness, contrast, saturation, auto black level compensation, auto white balance, auto exposure control and back light compensation.

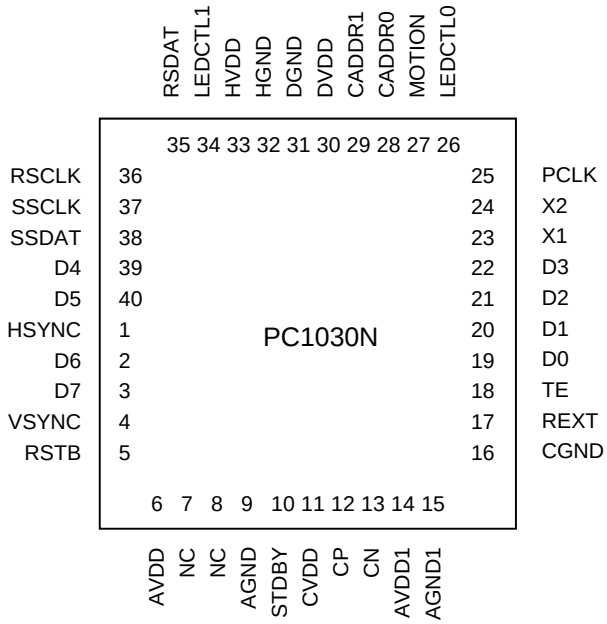
▷ Frame size, window size and position can be programmed through a 2-wire serial interface bus.

▷ VGA / QVGA / QQVGA / CIF / QCIF Scaling.

▷ 50Hz, 60Hz flicker automatic cancellation.

▷ High Image Quality and High low light performance.

▷ Internal Parking guide line
▷ AEC-Q100 Qualified




[ Fig. 1 ] PIN Description (40CLCC)

| | |
|---|---|
| Optical Format | 1/4 inch |
| Pixel Size | 5.55 um x 5.55 um |
| Effective Pixel Array | 648 x 488 |
| Effective Image Area | 3596.4um x 2708.4um |
| Clock Frequency | 27 MHz |
| Frame Rate | 60(50) fields/sec @ 27MHz |
| Sensitivity | 3.16 [V/Lux.sec] |
| Power Consumption | 213 [mW] @ Dynamic |
| | 19.2 [uW] @ Standby |
| Operating Temp. (Fully Functional Temp.) | -40'C ~ 105'C |

[ Table 1 ] Typical Parameters

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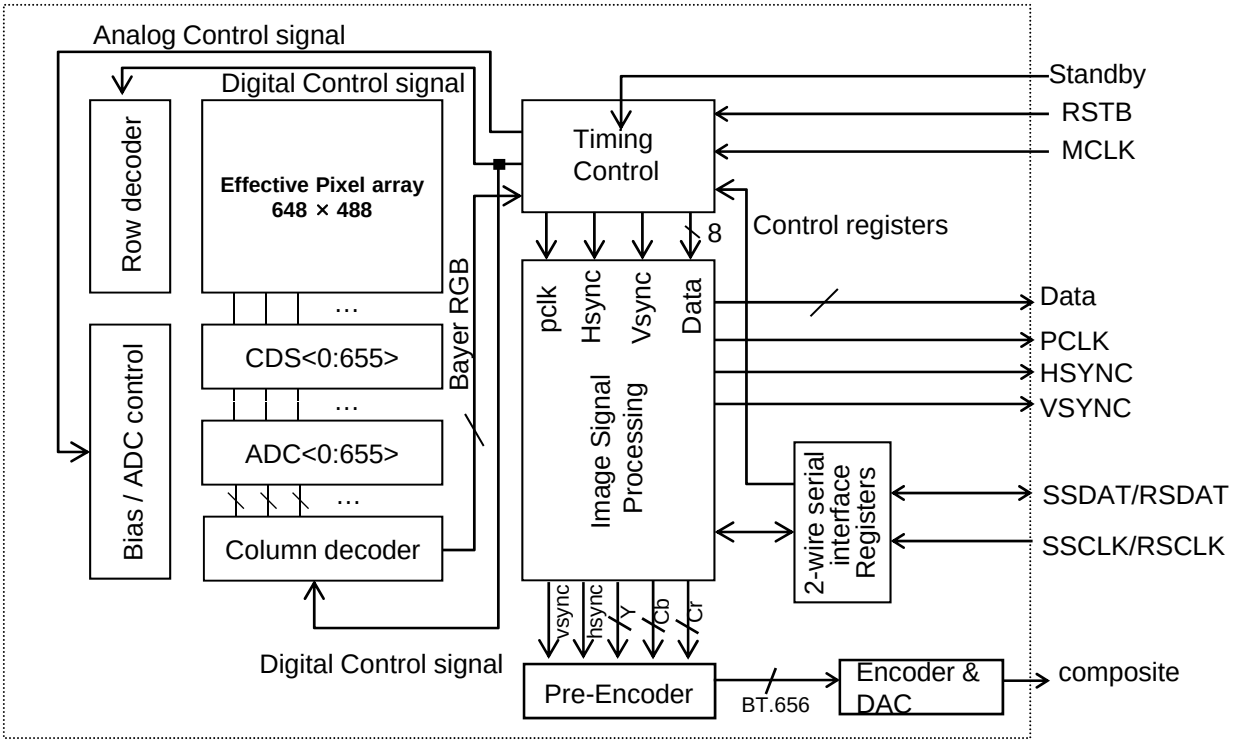
## ▶ Signal Environment

PC1030N has 3.3V tolerant Input pads. Input signals must be higher than or equal to HVDD but cannot be higher than 3.3V. PC1030N input pad has built in reverse current protection circuit, which makes it possible to apply input voltage even if the HVDD is disconnected or floating. Voltage range for all output signals is 0V ~ HVDD.

## ▶ Chip Architecture

PC1030N has 648 x 488 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing block and pre-encoder and encoder blocks to produce YCbCr 4:2:2 output data or composite output. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.




[ Fig. 2 ] Block Diagram